(iv) Relative

(v) Base register Addressing

(vi) Register indirect addressing (12)

(b) Demonstrate how interrupt is handled by drawing the memory diagram before and after the execution of an interrupt. (3)

7. (a) Differentiate between (attempt any **two**) :

(i) Programmed I/O and Interrupt driven I/O techniques

(iii) Main memory and Auxiliary memory

(iii) Isolated vs Memory mapped I/O (6)

(b) Explain data transfer from I/O device to CPU in programmed I/O with the help of suitable diagram and flow chart. (9)

[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 841

Unique Paper Code : 2342572301

Name of the Paper : Computer System Architecture

Name of the Course : **B.A. (Prog.) Computer Science**

Semester : III

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Question No. **1** in **Section-A** is compulsory.
3. Attempt any **4** questions from among questions **2** to **7** in **Section-B**.
4. Parts of a question must be answered together.

Section-A

1. (a) Give two instructions required to set E=1 in basic computer. (2)

(b) State and prove associative law on the following expression using truth table.

$AB + B'C + A'C$ (3)

(c) Which addressing mode is used to implement register-reference instructions. Justify your answer. (3)

(d) Show the representation of +8 and –7 in : (3)

(i) Signed Magnitude Representation

(ii) Signed 1's complement representation

(iii) Signed 2's complement representation

(e) Explain how ROM is different from RAM and give its applications. (3)

(f) The 8-bit registers AR, BR, CR, and DR initially have the following values: (4)

AR = 11110010

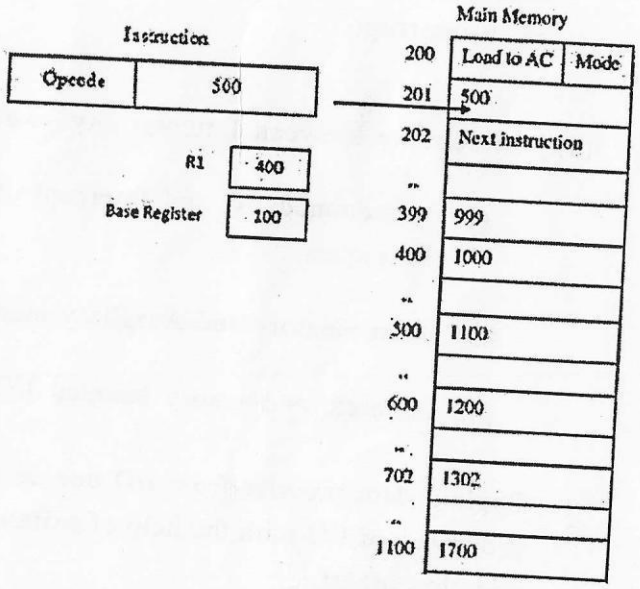
BR = 11111111

CR = 10111001

DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations.

The address field of the instruction is stored at address 201. The mode field specifies an addressing mode. R1 is the general purpose register, which has the value of 400. Base register contains the value 100.



Determine the effective address and the operand to be loaded for the following address modes :

(i) Direct

(ii) Immediate

(iii) Indirect

P.T.O.

(iii) Go over the instruction cycle to perform the above operation and give the contents of registers PC, AC, AR, DR, IR, I at the end of execute cycle.

5. (a) Covert the following decimal numbers to the base indicated. (2+2+2)

(i) 7562 to octal

(ii) 1938 to hexadecimal

(iii) 175 to binary

(b) Write the formula to find the (r–1)'s complement. Find the 7's complement of $(2345)_8$. (3)

(c) Perform the following arithmetic operations using 7-bit registers and detect the overflow, if any :

(+42) + (+33) and (–42) –(+33)

Use signed 2's complement representation for negative numbers. (6)

6. (a) A two-word instruction to perform the load operation is stored in memory at an address 200 as represented in the memory map given below.

CR ← CR^DR, BR←BR+1 AND DR to CR, increment BR

AR ← AR–CR Subtract CR from AR

(g) Implement OR and AND gates using only NAND gates. (4)

(h) Give reason why : (4)

(i) SC ← 0 is written at the end of execute sequence of all instructions.

(ii) IR ← M[PC] is not valid.

(i) Draw the diagram representing the I/O buses and Interface-modules. (4)

Section-B

2. (a) Given the Boolean function (10)

$F = xyz' + xy'z + x'y'z'$

(i) List the truth table of the function.

(ii) Draw the logic diagram using the original Boolean expression.

P.T.O.

(iii) Simplify the algebraic expression using Boolean algebra.

(iv) List the truth table of the function from the simplified expression and show that it is same as the truth table in part i.

(v) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part ii.

(b) Simplify the Boolean function F together with don't care conditions d in sum of products (SOP) form. Also draw the logic diagram of the simplified expression.

$F(w,x,y,z) = \Sigma(1, 2, 5, 7, 8, 10)$

$d(w,x,y,z) = \Sigma(3, 6, 11, 15)$ (5)

3. (a) The memory unit is specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed for 8 M X 32 memory unit? Also draw its diagram. (5)

(b) Explain the designing of a 2-to-4-line decoder implemented using NAND gates. (6)

(c) Explain 4-bit binary adder using the logic diagram. (4)

4. (a) Write the micro-operations for implementing the following memory reference instructions of basic computer.

(i) Direct STA

(ii) Indirect BUN

(iii) Direct ISZ (6)

(b) The content of PC in the basic computer is 2A8 (all numbers are in hexadecimal). The content of AC is 7E02. The content of memory at address 2A8 is 935C. The content of memory at address 35C is 07AB. The content of memory at address 7AB is 219 A. (9)

(i) What is the instruction that will be fetched and executed next?

(ii) Show the binary operation that will be performed in the AC when the instruction is executed.