Name of the Department: PHYSICS DEPARTMENT

Name of the Course: B.Sc. Hons.–CBCS_DSE

Name of the Paper: Physics of Devices and Communications

Semester: V- Semester

Unique Paper Code: 32227505

Question paper Set number: SET A

Total Marks: 75

Attempt four questions out of six. Each question carries equal marks.

1. (a) Explain the structure of Uni-Junction Transistor (UJT) along with the equivalent circuit. Derive the expression of intrinsic standoff ratio in UJT?
   (b) Explain the accumulation condition of MOS capacitor with the help of energy band diagram. Sketch the low-and high-frequency C-V characteristics of this capacitor, and explain their differences. How would the characteristics change at large negative gate bias if we doubled the oxide thickness? How about if we doubled the substrate doping?
   (c) Find the pinch off voltage in an n-channel JFET at 300K with a donor concentration of 2 x 10^{16} cm^{-3} and junction thickness of 8.75 μm. (Given dielectric constant of Si=12).
   5+10.75+3
2. (a) Discuss the rectifying and ohmic contacts. Draw the energy band diagram of an n-type semiconductor-metal diode under thermal equilibrium condition, assuming that the work function of metal is more in comparison to that of semiconductor.
   (b) With the help of schematic diagrams, describe the construction and working of MOSFET in Depletion and Enhancement mode. Discuss the expression of current-voltage for an ideal n-channel MOSFET.
   (c) Calculate the maximum width of the surface depletion region of a MOS diode having $N_A=8x10^{17}cm^{-3}$, $n_i=9.5x10^9$ cm^{-3}, dielectric constant of Si=11.9 and KT/q at room temperature=0.026 eV. 8+8+2.75

3. What is meant by Integrated circuits and how are they classified based on the number of components? What do you mean by metallization process? Define the process of Lithography? Explain two type of lithography techniques i.e. UV Lithography and E-beam Lithography. What is the need of impurity doping? 4+3+3+6.75+2

4. (a) What is phase-locked-loop (PLL), explain with block-diagram? What is locked condition in PLL? Make circuit diagram of VCO and also write formula for resonance frequency VCO.

(b) Explain the difference between first order and second order low pass filter based on the circuit and frequency response. 5+3+6.75+4

5. (a) Explain the significance of handshaking for digital data communication?
(b) Give detailed explanation of various lines and signals used in RS232 for serial communication.
(c) What is the advantage of using parallel communication over serial communication.
5+8.75+5

6. (a) Define amplitude modulation and modulation index. Derive an equation for amplitude modulated wave and draw its frequency spectrum. Obtain bandwidth, total voltage and total power in amplitude modulated wave.
(b) A single-tone FM is represented by the voltage equation as:

$$v_c(t) = 12\ \cos(6\text{x}10^8\ t + 5 \sin 1250\ t)$$

Determine the following: (i) carrier frequency, (ii) modulating frequency, (iii) the modulation index, (iv) maximum deviation and (v) what power will this FM wave dissipate in 10 Ω resistors.
(c) Discuss the demodulation of AM wave using diode detector. 10+5+3.75