Unique Paper Code	: 42344403
Name of the Course	: B.Sc. Physical Science/Mathematical Science
Name of the Paper	: Computer System Architecture
Semester	: IV
Duration	: 2 Hours
Maximum Marks	: 75
Year of Admission	: 2015, 2016 & 2017

Instructions for Candidates:

Attempt any four questions. All questions carry equal marks.

Q1. Describe various pros and cons of two-address and three-address instructions. Write down two separate programs to evaluate the following arithmetic expression using two address and three address instructions:

$$X = (C * D) * (E - F)$$

Also mention their corresponding micro-instructions in each of the two programs. Use the symbols ADD, SUB and MUL for arithmetic operations; MOV for the transfer-type operation; and LOAD and STORE for transfers to and from AC register and memory. Assume that memory operands are stored at memory addresses C, D, E and F and the result must be stored in memory at address X.

Q2. Given the Boolean function:

$$F = xy + x(yz + yz')$$

List the truth table of function F and draw its logic diagram. Further, simplify function F using Boolean algebra, draw the truth table of simplified version of function and show that it is same as earlier truth table. Draw the logic diagram from the simplified expression and compare the total number of gates with the earlier logic diagram.

Q3. Explain how can you represent signed binary numbers in digital computer? Convert the signed numbers (-75) and (-85) in binary form using following three representations- signed representation, one's complement representation and two's complement representation. Use 8-bit register to represent all these numbers. Perform following arithmetic operations in binary using signed 2's complement representation for negative numbers.

+85	-85
-75	-75
-----	-----
-----	-----

Also, identify in which of these cases overflow occurs and why.

Q4. Explain the role of multiplexor used in the common bus diagram of the Basic Computer Organization as shown below in Figure I. Consider the following register transfer statements to be executed in the system of Figure I. For each transfer, specify: the binary value that must be applied to bus select inputs S_2, S_1 and S_0, the register whose LD control input must be active and a memory read or write operation (if needed).
Also justify your answer in each of following register transfer statement.

Register Transfer statements

$DR \leftarrow M[AR]$, $TR \leftarrow M[AR]$(simultaneously)
$M[AR] \leftarrow IR$, $TR \leftarrow IR$(simultaneously)
$DR \leftarrow TR$, $IR \leftarrow TR$(simultaneously)
$M[AR] \leftarrow AC$, $DR \leftarrow AC$ (simultaneously)

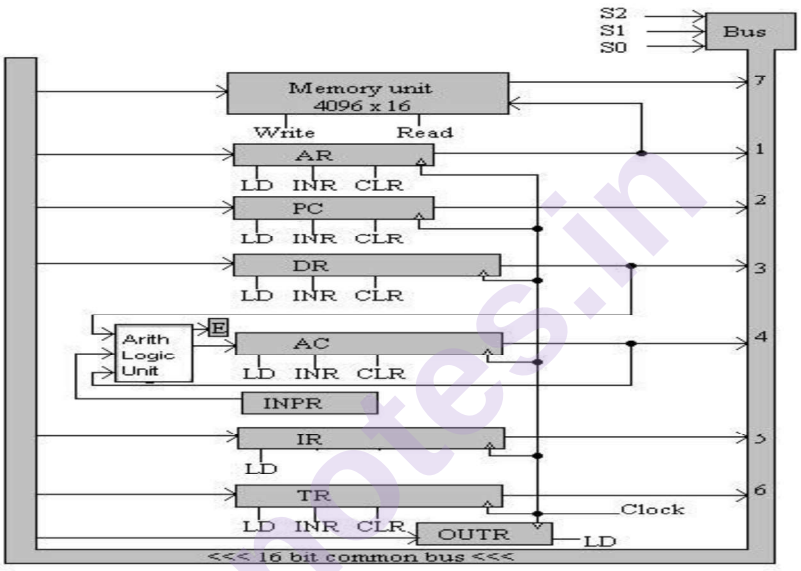

Figure I The Common Bus System

Q5. Design a combinational circuit with four inputs, w, x,y and z and four outputs A, B and C. When Binary inputs is 0,1,2, 3, 4, 5, 6 or 7 the binary outputs is three greater than the input. When the binary input is 8, 9, 10, 11, 12, 13, 14 or 15, the binary output is two less than the input. Solve the output functions A, B, C and D in sum of product form and draw the logic diagram for the same.

Q6. Explain how you can say that a register is a sequential circuit. Draw a block diagram of a 5-bit register using five D-flip-flops, five external input values I_0, I_1, I_2, I_3, I_4, five output values A_0, A_1, A_2, A_3, A_4, a common clock and a clear signal.
Assume that the following 10-bit registers R_1, R_2, R_3 and R_4, initially have the following unsigned values:

R_1=1100110011 R_2=1110001111
R_3=0011001111 R_4=0101010101

Determine the 10-bit values in each register after the execution of the following sequence of micro-operations:

$$R_1 \leftarrow \overline{R_1} + \overline{R_2}$$
$$R_2 \leftarrow R_3 \vee \overline{R_4}$$
$$R_4 \leftarrow (R_3 \vee \overline{R_4}) + R_1$$