B.E. Electronics & Telecommunication / Communication Engineering / Electronics Engineering
Eighth Semester

EN803 - Digital System Design

P. Pages : 2 **GUG/W/18/2019**

Time : Three Hours * 1 5 4 8 * Max. Marks : 80

Notes : 1. All questions carry equal marks.
2. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Explain Moore's law. **2**

b) What are the methods of design entry into a CAD system. **5**

c) What are the two HDL's used . **4**

d) Draw a flow chart for a typical VHDL CAD system. **5**

OR

2. a) What are standard Chips. **4**

b) What are PLD'S How are they superior to standard chips. **4**

c) What are the rules to be followed for selecting the name of the entity. **4**

d) Explain placement and routing. **4**

3. a) What are the different types of assignment statements used in VHDL. **4**

b) Write a VHDL code for a 4 to 1 multiplexer using selected signal assignment statement. **6**

c) Write a VHDL code for a 4 to 2 priority encoder using conditional signal assignment statement. **6**

OR

4. a) Write a VHDL code for a 4bit ALU. **5**

b) Write a VHDL code for a 2 to 4 binary decoder using case statement. **6**

c) Write a VHDL code for a 3 bit up counter. **5**

5. a) Design a sequence detector to detect a sequence of 30's using Moore circuits. Use D flipflops. Note that for the fourth zero, output should be zero. **8**

b) Design a Mealy synchronous circuit that yields output z = 1 during one clock cycle provided that there have been three one's in the input line during exactly the 3 preceding clock intervals. If there are one's during four or more cycles, output Z = 0. Use D flipflops. **8**

OR

6. a) Design a Moore synchronous circuit with a single input X and a single output Z. The circuit makes Z = 1 whenever exactly one pair of identical bits has been the input provided that the pair was preceded by exactly a pair and provided that bits in successive pairs are different use JK flipflops. **12**

b) Also write VHDL code for the above circuit **4**

7. A fundamental mode circuit has two inputs X_1 and X_0 and an output Z. when $X_1X_0 = 00$, the circuit has two stable states one with Z = 0 and one with Z = 1. If the circuit is in the state with Z = 0, a change to $X_1X_0 = 01$ and a return to $X_1X_0 = 00$ will cause a state change. Similarly, a change to $X_1X_0 = 10$ and a return to $X_1X_0 = 00$ will cause a reverse change of state. On the basis of this word description. of the required ckt performance, make a transition table. Make an arbitrary state assignment, and design the circuit. **16**

OR

8. A fundamental mode circuit has inputs X_1 and X_0 and a single output Z. When $X_1X_0 = 00, Z = 0,$ To make $Z = 1$, we start with $X_1X_0 = 00$ and first change X_0 to 1 and next change X_1 to 1. To return Z to Z=0 we must return $X_1X_0 = 00$, the order of return being of no consequence. **16**

a) Make a primitive flow table.

b) Eliminate redundant states if any.

c) Make a state assignment which avoids critical races.

d) Draw the logic circuit.

9. a) With the help of a schematic, Explain the operation of a PAL. **8**

b) Design a PAL for the following functions. **8**

$w(A,B,C) = \sum(1,2,5,6)$

$x(A,B,C) = \sum(0,1,4,5)$

$y(A,B,C) = \sum(1,5,6,7)$

$z(A,B,C) = \sum(0,1,6,7)$

OR

10. Write short notes on **any two.** **16**

a) PLA

b) CPLD.

c) FDGA.

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