B.E. Electronics & Telecommunication /
Communication Engineering / Electronics Engineering Seven Semester

EC7053 / EN 704 - Elective-I : VLSI Design

P. Pages : 2 **GUG/W/18/1799**

Time : Three Hours * 1 4 0 8 * Max. Marks : 80

Notes : 1. All questions carry equal marks.
2. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Describe the history of CMOS circuit. **4**

b) Implement a Nand gate using CMOS logic. **4**

c) Design a CMOS logic gates for the following function. **8**
i) $Z = \overline{A \cdot B \cdot C \cdot D}$
ii) $Z = \overline{A + B + C + D}$

OR

2. a) Design a 2 to 1 multiplexer using CMOS logic. **5**

b) Design a CMOS positive -level- sensitive D latch. **5**

c) Design a CMOS positive edge triggered D register. **6**

3. a) Explain the operation of an NMOS enhancement transistor in the cutoff, linear and saturated regions of its operation. **6**

b) Calculate the threshold voltage for an n transistor at 300°K for a process with Si substrate with NA = 1.80×10^{16} , a SiO_2 gate oxide with thickness 200 A° .
Assume $\phi ms = -0.9$ V, $\theta fe = 0$) . **6**

c) Explain Body effect. **4**

OR

4. a) Derive the expression for output voltage of a CMOS inverter in Region B of its operation. **7**

b) Explain the operation of transmission gate. **5**

c) Explain the operation of any one Bicros inverter. **4**

5. a) Explain the Czcharsui method of water processing. **8**

b) Explain the twin tub process of CMOS technology. **8**

OR

6. a) What are design rules. What are the issues they address. Write the layout rules. **10**

b) What is latch up. Explain with the help of a sketch. How is latch up problem avoided. **6**

7. a) Derive the expression for capacitance in the cutoff linear and saturated regions. What is the total capacitance. **8**

b) Derive the expression for full time for a CMOS inverter. **8**

OR

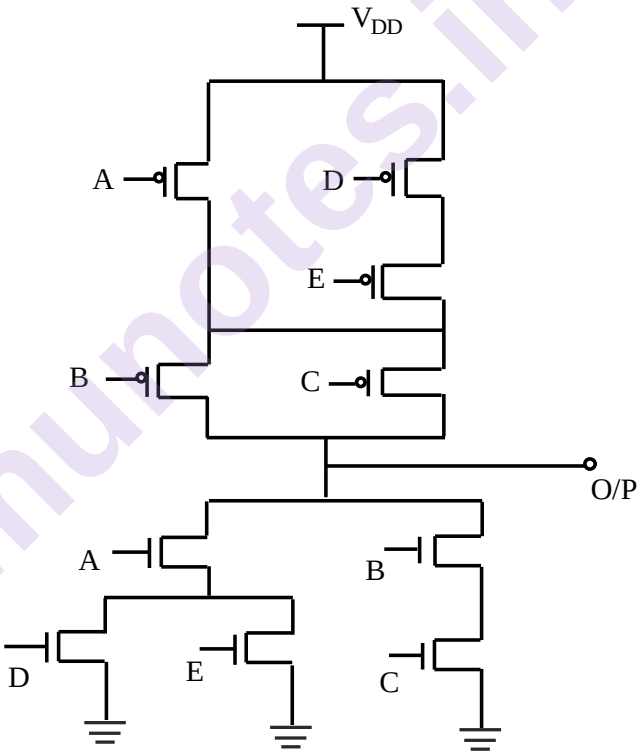
8. a) Derive the expression for short cut dissipation for a CMOS inverter. **8**

b) Describe charge sharing hence derive expression for QT, CT and VR. **4**

c) A pre charge bus has a loading of 10pF. At a point in the clock cycle, 64 registers with transmission gates on their inputs turn on. The input load of each register (after the transmission gate) is 0.1 pF. calculate change in precharge voltage. **4**

9. a) Draw a physical layout of an inverter. **6**

b) For the cut diagram given draw a physical layout using Euler graph. **10**



OR

10. Write short notes on **any two.** **16**

a) CMOS logic structures.

b) Clocking strategies.

c) Yield

d) Static load MOS inverter.

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