B.E. Instrumentation Engineering Fourth Semester

# IN405 - Digital Circuits

P. Pages : 2 **GUG/W/18/1578**

Time : Three Hours * 1 2 4 2 * Max. Marks : 80

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Notes : 1. Same answer book must be used for each section.
2. All questions carry marks. as indicated.
3. Due credit will be given to neatness and adequate dimensions.
4. Assume suitable data wherever necessary.
5. Diagrams and Chemical equation should be given wherever necessary.

**1.** a) Verify the following operations are cumulative but not associative **6**
i) NAND ii) NOR

b) Perform the following. **6**
a) $(492)_8 = (?)_{16}$
b) $(1011101)_{Gray} = (?)_{B.}$
c) $(49)_D - (62)_D$ using 2's complement method.

c) State & prove D' Morgan's Law. **4**

**OR**

**2.** a) Design binary to gray code converter using logic gates. **8**

b) Realize AND, OR, NOT, Ex-OR Gates using NAND Gates Only. **6**

c) Write the advantages of 2's compliments over 1's compliments. **2**

**3.** a) Draw & explain CMOS circuits for NOR gate. **8**

b) For an open-collector TTL gate the specifications are. **8**
$V_{OH} = 2.4V,\ V_{OL} = 0.4V, I_{OH} = 250\ \mu A$
$I_{OL} = 16\,MA, I_{IH} = 40\ \mu A, I_{IL} = -1.6\,MA$
if 5 such gates are wire - AND ed, and are loaded by similar 6 gates, calculate the value of collector resistor $R_C$ required. Assume $V_{CC} = 5V$.

**OR**

**4.** a) Define the following terms. **6**
i) Fan - in ii) Fan - out
iii) Propagation Delay iv) Noise Margin

b) Explain the ECL logic family with neat sketch. **7**

c) Compare decoder with a Demultiplexer. **3**

**5.** a) I) Make K - map for the function. **6**

$$f = AB + A\bar{C} + C + AD + A\bar{B}C + ABC$$

II) Express f in standard SOP form.

III) Minimize it and realize the minimized expression using NAND gates only.

b) Design half adder & full adder with logic Ckt and K-map. Explain concept of carry look ahead adder. **10**

**OR**

**6.** a) Write the difference between **6**

i) MUX and DEMUX

ii) Encoder and Decoder.

b) Explain octal to binary encoder with suitable truth table. **6**

c) Simplify using K - map. **4**

$$F(A, B, C, D) = \pi M\,(4, 6, 10, 12, 13, 15)$$

**7.** a) Differentiate between synchronous and asynchronous counters. Draw & explain 3-bit synchronous counter. **8**

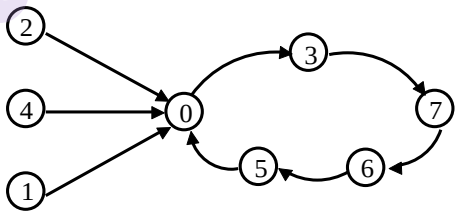
b) Explain the J-K flip flop with logic gate circuit & excitation table. **8**

**OR**

**8.** a) Convert JK Flip-Flop into T-Flip-Flop. **8**

b) Illustrate 3-bit ripple up counter using negative edge triggering. **8**

**9.** a) Design a lock free counter for the following states. **8**




b) Discuss the function of FPGA with necessary diagram. **8**

**OR**

**10.** a) Design a counter of arbitrary modulo with k-maps. **8**

b) Explain VHDL with necessary diagram. **6**

c) What is programmable logic Device (PLD) **2**

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