B.E. Electronics & Telecommunication / Communication Engineering
Third Semester (Old) CBS Pattern

ET 304 - Digital Electronics

P. Pages : 2 **GUG/W/18/1496**

Time : Three Hours * 1 1 8 0 * Max. Marks : 80

Notes : 1. All questions carry equal marks.
2. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) What are the advantages of digital circuits over analog circuits. **5**

b) State and prove DeMorgan's theorem for 3 variables. **5**

c) Perform the following operation : **6**
i) Convert $(675.625)_{10}$ to hexadecimal
ii) Convert $(574.321)_8$ to binary
iii) Convert $(6327.4051)_8$ to decimal

OR

2. a) Minimize the following Boolean functions using kmaps **8**
i) $f(A, B, C, D) = \sum m (0, 2, 3, 4, 5, 7, 8, 9, 13, 15)$
ii) $f(A, B, C, D) = \prod M (1, 2, 4, 5, 7, 8, 10, 11, 13, 14)$

b) Minimize the following Boolean function using Quine Mc Cluskey method. **8**
$f(w, x, y, z) = \sum (1, 4, 6, 7, 8, 9, 10, 11, 15)$

3. a) Define the following term : **10**
i) Fan in
ii) Fan out
iii) Noise margin
iv) Propagation delay
v) Power dissipation

b) Explain the operation of a TTL Nand gate. **6**

OR

4. a) Explain the operation of CMOS Nand CMOS Nor gate. **8**

b) What is Tristate logic. What are the difficulties encountered, when driving many number of gates. How is this overcome using a TSL inverter. Explain. **8**

5. a) Design a logic circuit with 4 inputs A, B, C, D to generate an output Z which is active if one or the other but not both of the following conditions are satisfied. **8**
i) Both inputs A and B are active
ii) Either C or D or both are active

b) Design a BCD to excess 3 code converter. **8**

OR

6.	a)	Design a 5x32 decoder with 4 line 3x8 decoder and a 2x4 decoder.	**8**
	b)	Explain the working a 8 to 1 multiplexer with the help of a schematic.	**8**
7.	a)	Differentiate between synchronous and asynchronous sequential circuits.	**8**
	b)	What is race around condition in SR flip flop. How is this problem over came using master slave JK flip flop.	**8**

OR

8.	a)	Design a 3bit up down counter using JK flip flops.	**12**
	b)	Convert a JK filp flop to a D flip flop.	**4**
9.	a)	Explain the following terms in VHDL. i) Entity ii) Architecture	**6**
	b)	Explain structural modelling, data flow modelling and behavioural modelling in VHDL.	**10**

OR

10.		Write short notes on **any two.**	**16**
	a)	CPLD	
	b)	FPGA	
	c)	RAM	
	d)	ROM	

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