Bachelor Of Science (B.Sc.-III) Fifth Semester

B.Sc. 3516 - Electronics Paper-I (Compulsory)
(Microprocessor, Interfacing & PPI Devices)

P. Pages : 1 **GUG/W/18/1306**

Time : Three Hours * 1 0 1 9 * Max. Marks : 50

Notes : 1. All questions are compulsory and carry equal marks.
2. Draw neat and labelled diagram wherever necessary.

1. EITHER:-

a) Draw a block diagram of 8085 microprocessor. **5+5**
Explain the function of following flags:-
i) Carry status (CS) ii) Auxiliary carry (AC)
iii) Zero flag (Z) iv) Parity flag (P)
v) Sing flag (S)

OR

b) Explain the following **5+5**
i) Fetch Operation ii) Execution Operation

2. EITHER:-

a) What is an addressing mode? Explain register indirect and implicit addressing mode with suitable examples. **6+4**
Explain the meaning of any two following instructions.
i) SBBr ii) ADDc iii) ADI data

OR

b) State various groups of instruction set in 8085 μ_p with one example of each. Write an ALP to perform addition of three 8-bit numbers stored in memory location 6500H, 6501H, 6502H. **5+5**

3. EITHER:-

a) What is interfacting? Explain the needs of interfacing. **4+6**
Explain
i) Memory mapped I/O scheme ii) I/O mapped I/O scheme.

OR

b) Explain programmed data transfer scheme in 8085 μ_p. **5+5**
Explain burst mode and cycle staling in DMA data transfer scheme.

4. EITHER:-

a) Draw the block diagram of 8255 PPI. **4+6**
Explain any two operating modes of 8255 PPI.

OR

b) What is DMA controller? Explain schematic diagram of programmable DMA controller 8257. **2+8**

5. a) Explain timing and control unit in 8085 μ_p. **2½**

b) Write a programme in ALP to find 1's complement of 8 bit data. **2½**

c) Explain interrupt driven data transfer scheme. **2½**

d) Draw schematic diagram of Programmable Interval times 8253. **2½**

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