B.E. Electronics & Telecommunication / Communication Engineering (CBCS Pattern)
Third Semester

3BEET02 - Digital Electronics

P. Pages : 2 **GUG/W/18/11497**

Time : Three Hours * 3 5 8 2 * Max. Marks : 80

Notes : 1. All questions carry equal marks.
2. Illustrate your answers wherever necessary with the help of neat sketches.

1. a) Do as directed. **8**

i) $(121.21)_{10} = (\quad)_8$

ii) $(345.345)_{10} = (\quad)_{16}$

iii) $(6021.15)_{16} = (\quad)_{10}$

iv) $(505.16)_{16} = (\quad)_8$

b) State and prove DeMorgan's theorem for 3 variables. **4**

c) Simplify using k map **4**
$f = ABC + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + AB$

OR

2. a) Minimize using k maps. **8**
f(A, B, C, D) = $\sum$ m (0, 2, 3, 5, 7, 8, 9, 10, 11, 13, 15)
f(A, B, C, D) = $\prod$ M (3, 5, 7, 9, 11, 15) + d(0, 13, 14)

b) Minimize using Quine McCluskey method. **8**
f = $\sum$ (1, 2, 3, 6, 7, 8, 10, 11, 12, 14, 17, 18, 20, 21, 22, 24, 28)

3. a) Draw & explain TTL Nand gate. **8**

b) Explain the salient features of TTL. **8**

OR

4. a) Explain the following term. **8**

i) Fan in ii) Fan out

iii) Propagation delay iv) Power dissipation

b) Implement Nand & NOR gates using CMOS. **8**

5.	a)	Design a even parity generator and checker.	**8**
	b)	Design a 4 bit digital comparator.	**8**

OR

6.	a)	Design a 16 to 1 multiplexer using 5 4 to 1 multiplexer.	**8**
	b)	Design a priority encoder with D3 having the highest priority followed by D2, D0, D1.	**8**
7.	a)	Explain the operation of SIPO shift register.	**8**
	b)	Convert a SR flip flop to a JK flip flop.	**8**

OR

8.	a)	Design a synchronous decade counter using D flip flops.	**8**
	b)	Design a counter that is Lockfree and steers through the states S0, S2, S4, S6, S7. Use JK flip flop.	**8**
9.	a)	Explain in brief SRAM, ROM, EPROM and flash memory.	**8**
	b)	Explain PLA with suitable example.	**8**

OR

10. Write notes on **any two.** **16**

a) ADC

b) DAC

c) Sample and hold circuit.

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