B.E. Electrical (Electronics & Power) Engineering / Electronics Engineering / Electronics & Telecommunication / Comm. Engineering (CBCS Pattern) Third Semester CBCS (New)

3BEEE04 / 3BEEN02 / 3BEET03 : Electronics Devices & Circuits

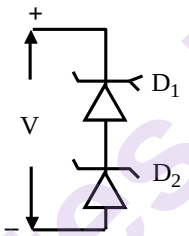
P. Pages : 3 **GUG/W/18/11489**

Time : Three Hours * 3 5 7 4 * Max. Marks : 80

Notes : 1. All questions carry marks as indicated.
2. Due credit will be given to neatness and adequate dimensions.
3. Assume suitable data wherever necessary.

1. a) Derive the V – I relationship of P – N Junction diode. **8**

b) The saturation currents of two Zener diodes in the circuit are $1\mu A$ and $2\mu A$ respectively. **8**
The break down voltages of the diodes are same and equal to 100V.
Calculate the current and voltage of each diode if $V_i = 90V$ & $V_i = 110V$.



OR

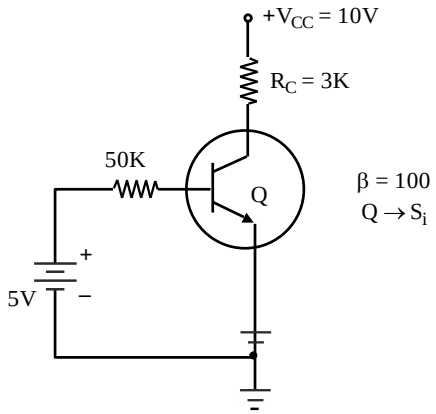
2. a) Explain how depletion layer is formed across P – N Junction. Define barrier potential? **4**

b) Explain Zener diode as voltage regulator. **4**

c) A, 120V, 60Hz voltage is applied to primary of 5:1 step-down transformer whose secondary is centre-tapped allowing a load of $1K\Omega$ be connected to a full-wave rectifier utilizing two diodes. Neglecting voltage drop across two diodes. Determine : **8**
i) The d.c. voltage across the load.
ii) d.c. current through the load.
iii) % efficiency.
iv) PIV of each diode.

3. a) Explain Base – Width modulation in BJT. **4**

b) For the ckt shown in fig. **8**



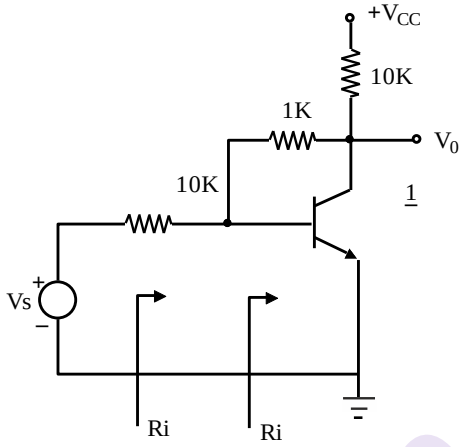
Show that Q is working in Saturation region. Also find currents.

c) What is mean by biasing? Why there is need of biasing? Explain. **4**

OR

4. a) Derive the hybrid parameters for. C – E configuration and draw the hybrid model. **8**

b) For the ckt shown in fig. **8**
Find AI & A_{VS}.



5. a) Define thermal resistance & Derive the expression for condition of thermal stability in self bias ckt. **8**

b) A Si- transistor with $\beta = 50,\ V_{BE(act)} = 0.7V,\ V_{CC} = 22.5V \& R_C = 5.6K\Omega$ is used in voltage divider bias ckt. It is desired to establish Q. pt. at $V_{CE} = 12\,V \&\ I_C = 1.5\,mA$. For stability factor $S \le 3$, find $R_1,\ R_2, \&\ R_e$. **8**

OR

6. a) Draw the hybrid π- model of BJT in C – E connection & derive the expression for current gain. **8**

b) A BJT has $g_m = 25m\mho,\ rb'_e = 4.9K, h_{ie} = 5\Omega, rbb' = 100\,\Omega, cb'_c = 10\,pf,\ cb'_e = 60\,pf$ and $h_{fe} = 224$ at 1KHz. Calculate α and β cut-off frequencies and f_T. **8**

7. a) Differentiate between MOSFET and JFET. **4**

b) For JFET, if $I_{DSS} = 20mA,\ V_{GS(off)} = -5V$ and $g_{mo} = 4\,mS$. **4**
Determine transconductance for $V_{gs} = -4V$ and I_D at that point.

c) The amplifier shown has $V_P = -2V,\ I_{DSS} = 1.65\,mA$. It is desired to bias the ckt at $I_D = 0.8\,mA$ using $V_{DD} = 24\,V$. Assume $rd >> Rd$, find $V_{gs},\ g_m, R_s \& R_d$ such that the voltage gain is at least 60 dB with R_s by passed with very large capacitance. **8**

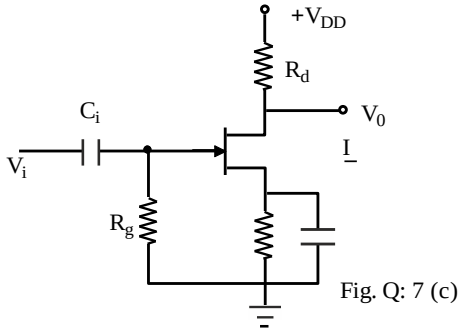
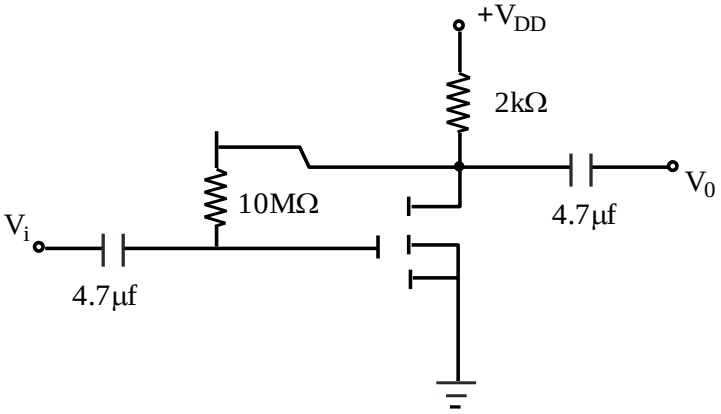


Fig. Q: 7 (c)

OR

8. a) Explain the effect of temperature in MOSFEET with neat waveform. **8**

b) For the ckt shown below given that $I_{D(ON)} = 6\,mA$, $V_{GS(ON)} = 8V, V_{gs(th)} = 3V$. **8**
Calculate the values of I_D and V_{GS} at $Q-$ point.



9. a) Draw the ckt of class B-push-pull amplifier. Obtain the condition for maximum power dissipation and hence show that $P_{c(max)} = 0.4 P_{o(max)}$. **8**

b) A transistor supplies 1W to $5K\Omega$ load. A zero signal d.c. collector current is 35 mA and d.c. collector current with signal is 40 mA. Determine % second harmonic distortion. **8**

OR

10. a) With neat ckt diagram, explain transformer, coupled class A push-pull Amplifier, how removes the problem of core saturation and eliminate even harmonics completely. **8**

b) Class B push pull amplifier is supplied with $V_{CC} = 60V$ and signal to collector voltage down to $V_{min} = 15V$. The dissipation in both transistor totals 45W. Find : **8**

i) Load presented by O/P transformer.
ii) Conversion efficiency.
iii) Ratings of each transistor.

****