

**EP502 - Microprocessors and Microcontroller**

P. Pages : 2

Time : Three Hours



**GUG/W/16/3721**

Max. Marks : 80

- Notes :
1. All questions carry marks as indicated.
  2. Due credit will be given to neatness.
  3. Assume suitable data wherever necessary.
  4. Illustrate your answers wherever necessary with the help of neat sketches.
  5. Use of slide rule, Drawing instruments and non programmable calculator is permitted.
  6. All questions are compulsory. However the students may avail internal choice.

1. a) Draw the Architectural diagram of 8085 A  $\mu$ p . **10**
- b) Explain Flag structure of 8085 $\mu$ p . **6**

**OR**

2. a) Draw the timing diagram of MOV B, M instruction. **6**
- b) Explain what do you understand by Fetch, decode and execute operation. **6**
- c) Specify the number of T – states and machine cycles required for the following instructions : **4**

- i) XCHG                      ii) DADB
- iii) PUSH PSW              iv) RET

3. a) What the following instructions do in 8085? **4**
- i) XTHL                      ii) RST 1
- iii) RAL                      iv) JN 2 6060 H

- b) State similarities and difference between CALL & RET Vs. PUSH & POP instructions. **6**
- c) Find the 2's compliment of 16 bit number present in HL pair. Store the result in 6050 H and 6051 H memory locations. **6**

**OR**

4. a) Write a subroutine to create a delay of 5 milisecond. Also calculate the value of COUNT required for the above delay time. **8**
- b) Specify the contents of registers and flag status as the following instructions are executed. **4**
- MVI A, 00 H  
MVI B, F 8 H  
MOV C, A  
MOV D, B  
ADD D  
HLT

