M. Tech (with Credits)-Regular-Semester 2012
Computer Science and Engineering Sem III

CSE 1104 - Self Study-I

P. Pages : 1 **GUG/W/16/3825**

Time : Three Hours * 3 6 3 9 * Max. Marks : 70

Notes : 1. All questions carry equal marks.
2. Illustrate your answers wherever necessary with the help of neat sketches.
3. Due credit will be given to neatness and adequate dimensions.
4. Assume suitable data wherever necessary.

1.	a)	Discuss in brief a statically scheduled superscalar MIPS processor.	**7**
	b)	Explain control dependences.	**7**
2.	a)	Explain cache coherence problem.	**5**
	b)	Draw block diagram of sony playstation 2 and explain working of emotion engine in it. Also explain two modes of emotion engine organization.	**9**
3.		Explain the four general techniques of cache hit time reduction.	**14**
4.	a)	Does average memory access time due to cache misses predicts processor performance? Justify your answer by giving an example.	**7**
	b)	Explain segmented virtual memory protection in intel Pentium.	**7**
5.	a)	How Co-ordination is maintained in large distributed systems? Explain in brief.	**8**
	b)	Discuss issues in multiprocessor operating system.	**6**
6.	a)	What is object oriented software architecture? Explain in brief.	**5**
	b)	Sketch and explain the suitable architectural pattern for airline reservation system.	**9**
7.	a)	Explain in brief analysis model and design model.	**8**
	b)	What should be contents of good architectural model?	**6**
8.	a)	Discuss limitations of ILP.	**6**
	b)	Explain spin lock & steep lock in multiprocessor system.	**8**

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