Paper / Subject Code: 51402 / Logic Design

(**3 Hours**)

Questions No. 1 is compulsory.

N.B.:

1)

Please check whether you have the right question paper.

Q. P. Code: 37943

(Total Marks: 80)

		2)	Solve any three question out of remaining five questions.	
		3)	Assume suitable data if necessary .	
		4)	Figures to the right indicate full marks.	SP SAL
1	Solve any four out of five :		(20)	
	a)	W	hy biasing is necessary in BJT amplifier?	
	b)		lve (35) ₁₀ – (47) ₁₀ using two's compliment method.	
	c)	De	Define:	
	,		i) truth table	VK B
			ii) standard SOP	
			ii) De-Morgan's theorem	J. V.
			v) Duality theorem	
	4)		v) universal gate	2,
	d)		efine multiplexer and state its application.	
	e)	C	onvert S-R flip-flop to T flip-flop.	
2.	a)	Usir	g Quine-Me-dusky method determine minimum SOP form for	(10)
		f(x)	A, B, C, D) = $\sum m(0, 1, 3, 7, 8, 9, 11, 15)$	
	b)		at do you mean by differential amplifier? What is its primary function? State erent configurations of it, which one is popularly used.	(10)
3.	a)	Drav	w & explain Ring counter using suitable waveforms.	(10)
	b)	Imp	ement the following using only one 4:1 MUX and few gates:	(10)
		f(A, B, C, D) = $\sum m(0, 1, 3, 4, 5, 7, 9, 10, 12, 15)$	
4.	a)	Desi	gn MOD-9 Synchronous counter using J-K flip-flop.	(10)
	~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~		gn four bit BCD adder using IC7483.	(10)
	BUN	47.0		` ′
5.	a)	Wha	at is shift register? Mention different modes of operation of shift register?	(10)
	100	N 25 1	e and explain various VHDL data objects in brief.	(10)
	Cale		following (A say Posta)	(20)
	2	10 C	following (Any Four):	(20)
	a)	DO CY	HDL program format.	
	(b)	311	fference between combinational circuit and sequential circuits.	
	(c)	100 11	fferent biasing methods.	
	d)		ce-around condition in flip-flop.	
	e)	N-02- 2	rrent mirror circuit.	
à 2	f)	Ai	ithmetic logic unit.	