(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

1. Attempt **any four** **(20)**
   a) Compare constant voltage scaling and full voltage scaling.
   b) Compare single ended and differential power amplifiers.
   c) Why folded cascode is very popular building block in CMOS amplifier? Explain its advantages over double cascade.
   d) Derive output resistance of MOS current source.
   e) What are the advantages of active load?

2. a) Design an NMOS current source to provide a bias current of $I_Q = 100\,\mu A$ and an output resistance greater than 20 MΩ. The reference current is to be $I_{ref} = 150\,\mu A$. The circuit is to be biased at $\pm 3.3\,V$ and the voltage at the drain of the current source transistor is to be no smaller than $-2.2\,V$. The minimum width to length ratio of transistor is to be unity. **(12)**
   b) Explain cascade current mirror in detail. **(08)**

3. a) For CS amplifier with current source load find intrinsic gain A_o and explain the effect of output resistance on gain. **(10)**
   b) For CS stage with resistive load amplifier prove that Gain $= -g_m r_d$. **(06)**
   c) Compare double cascade with folded cascade. **(04)**

4. a) Explain PMOS fabrication process with suitable diagrams. **(10)**
   b) Explain with proper diagram CLASS F power amplifier. **(10)**

5. a) Explain in detail fabrication of transformer. **(10)**
   b) Explain short channel effects in MOSFET. **(10)**

6. a) Explain DC transfer characteristics of MOS differential amplifier. **(10)**
   b) Calculate the DC characteristics of MOSFET differential amplifier shown in Fig. 6(b) the transistor parameters are $k_{n1} = k_{n2} = 0.1\,\frac{\text{mA}}{\text{V}^2}$, $k_{n3} = k_{n4} = 0.3\,\frac{\text{mA}}{\text{V}^2}$, and for all transistor $\lambda = 0$ and $V_{tn} = 1\text{V}$. Determine the maximum range of common–mode input voltage. **(10)**

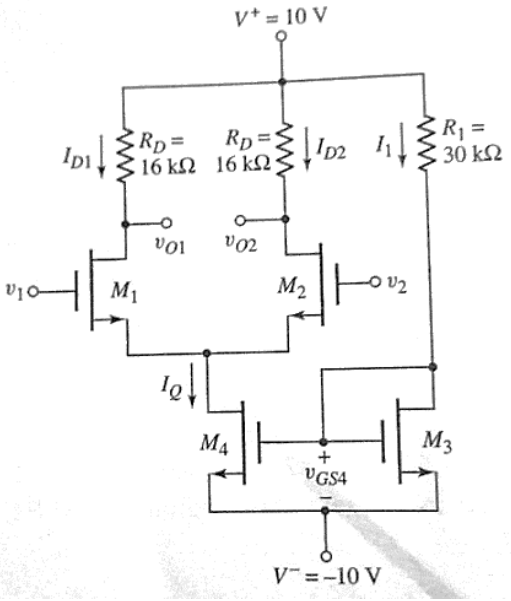

Fig. 6(b)