(3 Hours) **Max. marks: 80**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from the remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if necessary and mention the same in answer sheet.

Q.1 Attempt **any 4** questions [20]

(a) List the steps involved in fabrication process of MOSFET.
(b) Compare the output resistance of the cascade MOSFET current source to that of the two-transistor current source. Assume $I_{REF} = I_O = 100$ µA in both the circuits, $\lambda = 0.01$ V^{-1} for all transistors, and $g_m = 0.5$ mA/V.
(c) Draw a mask layout of NMOS transistor.
(d) Derive the equation for output resistance of common gate amplifier.
(e) Draw the equivalent model for transformer and explain.
(f) List the second order effects in MOSFET. Discuss any one of them.

Q.2 (a) Why is scaling required? Discuss the various types of scaling. [10]
(b) Consider the MOSFET current source in Fig. 2 (b) with $V^+ = 10$ V and $V^- = 0$, and the transistor parameters are: $V_{TN} = 1.8$ V, ½ $\mu_n C_{ox} = 20$ µA/V^2, and $\lambda = 0.01$ V^{-1}. The transistor width-to-length ratios are: $(W/L)_2=6$, $(W/L)_1=12$, $(W/L)_3=3$. Determine (i) I_{REF}, (ii) I_O at $V_{DS2} = 2$ V. [10]

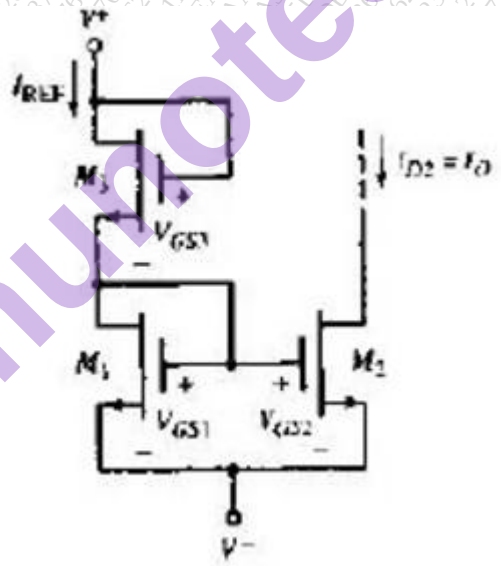

Fig. 2(b)

Q.3 (a) Consider the differential amplifier shown in Fig. 3(a). The transistor parameters are: $K_{n1}=K_{n2}=0.1$ mA/V^2, $K_{n3}=K_{n4}=0.3$ mA/V^2, and for all transitors, $\lambda=0$ and $V_{TN}= 1$ V. Determine the maximum range of common-mode input voltage. [10]

P.T.O

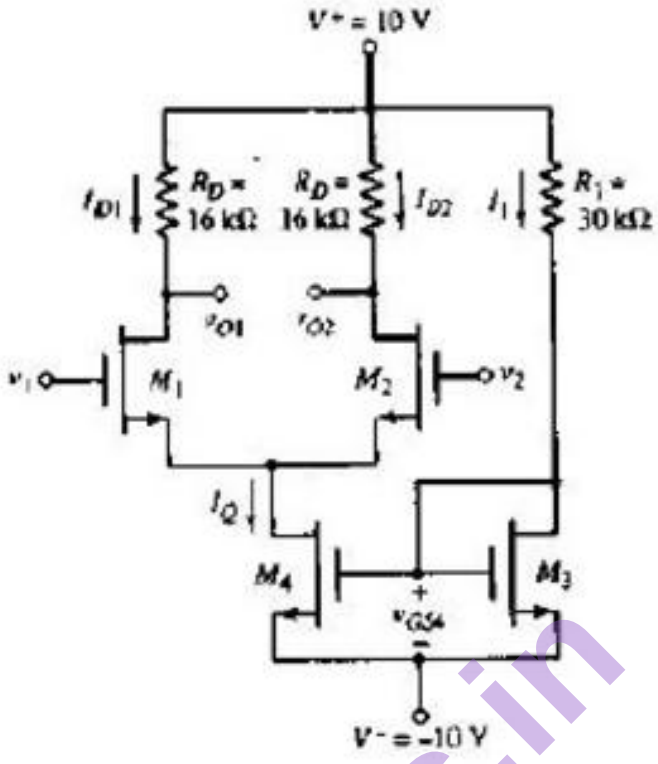

Fig. 3(a)

(b) With a neat circuit explain Bias Independent Current Source using MOSFET. [10]

Q.4 (a) For the circuit shown in Fig. 4(a), let $V_{DD} = V_{SS} = 1.5$ V, $V_{TN} = 0.6$ V, $V_{TP} = -0.6$ V, all channel lengths = 1 µm, $k_n' = 200$ µA/V^2, $k_p' = 80$ µA/V^2, and $\lambda = 0$. For $I_{REF} = 10$ µA, find the widths of all transistors to obtain $I_2 = 60$ µA, $I_3 = 20$ µA, and $I_5 = 80$ µA. It is further required that the voltage at the drain of Q_2 be allowed to go down to within 0.2 V of the negative supply and that the voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply. [10]

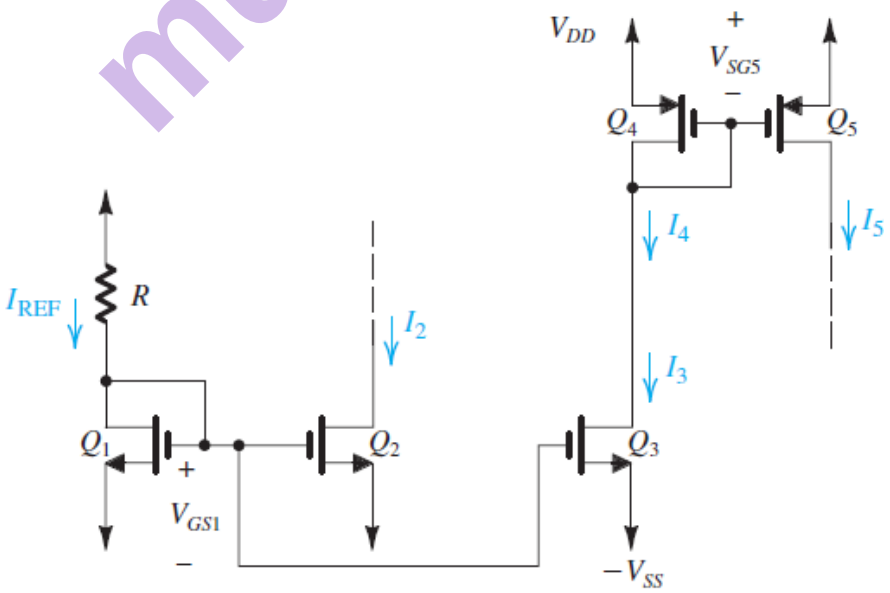

Fig. 4(a)

P.T.O

(b) Draw a small signal equivalent structure of Diff-amp and derive the equation for its CMRR. [10]

Q.5 (a) Draw a neat diagram of Class B power amplifier. Derive equation for its efficiency. [10]

(b) A CS amplifier utilizes an NMOS transistor with L=0.36 µm and W/L=10; it was fabricated in a 0.18-µm CMOS process for which $\mu_n C_{ox}$ = 387 µA/V^2 and V_A' = 5 V/µm. Find the values of g_m and A_0 obtained at I_D = 10 µA. [10]

Q.6 Short notes on: **(Attempt any four)** [20]

(a) Short channel effects in MOSFET.
(b) Wilson Current Mirror.
(c) MOS device capacitances.
(d) Folded cascode MOS amplifier.
(e) Fabrication of inductors.

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