Max. Marks: 80

N.B.: (1) Question No. 1 is compulsory. Solve any three questions from the remaining five (2) Figures to the right indicate full marks (3) **(4)** Assume suitable data if necessary and mention the same in answer sheet. Q. 1. Solve any four Questions out of five a) Perform the following operation using 2's compliment i) $(35)_{10} - (45)_{10}$ ii) $(45)_{10} - (35)_{10}$ Comment on results of (i) and (ii) В [5] If $F(A,B,C) = \sum m(1,3,4,5,6) + d(0,2)$ with its truth table and express F in SOP and POS form Convert D flip flop to T flip flop. \mathbf{C} [5] D **Explain Static RAM** [5] \mathbf{E} Design Full Adder using VHDL [5] Q. 2. Solve the following Prove that NAND and NOR gates are Universal gates [10] Convert the following into BCD and OCTAL code B [10] i) $(7AB)_{16}$ ii) (125)₁₀ Q.3. Solve any Two Questions out of Three Draw and explain a neat circuit diagram of BCD adder [10] Design a 3 – bit synchronous counter using J-K FLIP-FLOPs B [10] Realize the following functions of four variables using 8:1 multiplexer [10] $F = \Sigma m(0, 1, 2, 3, 7, 9, 10, 11, 13, 14, 15)$ Q. 4. Solve the following What are shift registers? How are they classified? Explain working of SISO [10] type of shift register. В Explain Full Adder circuit using PLA having three inputs, 8 product terms [10] and two outputs. Q. 5. Solve the following Draw and explain 4- bit Johnson counter [10] B Draw and explain 3 bit asynchronous binary counter using positive edge [10] triggered JK flip flop. Q. 6. Solve the following Compare TTL and CMOS logic families [05] Convert the following equation in its Canonical form B [05] $Y = AB(C + \overline{C}) + A\overline{C}(B + \overline{B}) + BC(A + \overline{A})$ Simplify the following expression using Boolean algebra [05] Y (A,B, C) = Σ m(0,1,2,3,4,5,6,7) Compare Moore and Mealy Machine with neat Diagram [05]

Time: 3 Hours