

Note: 1) Question no. 1 is compulsory.

2) Solve any three questions out of remaining.

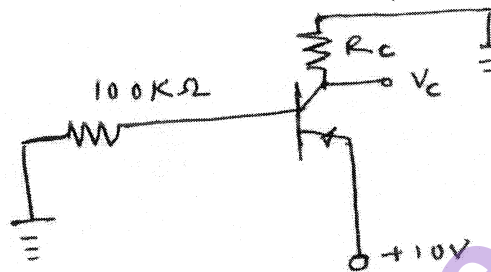
3) Fig. to the right indicates maximum marks.

4) Assume suitable data wherever necessary but justify the same.

Q1. Solve any five.

(5x4 = 20)

a) Determine the value of R_c such that $V_c = 5V$ and $\beta = 50$.

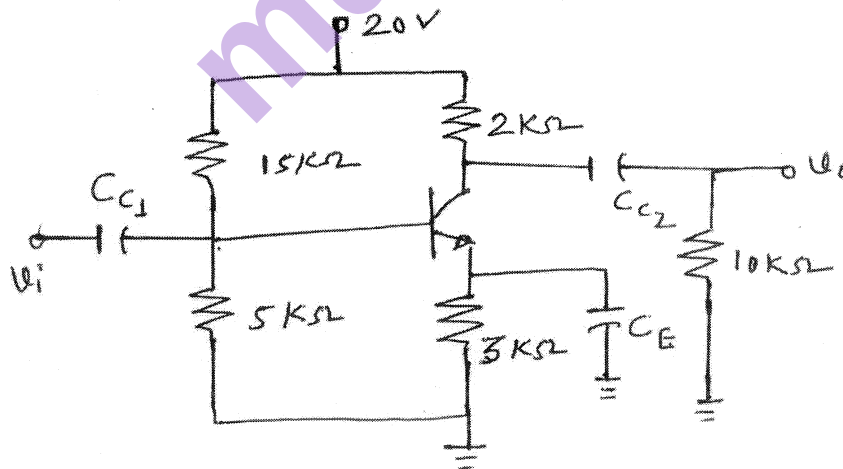


b) State and explain Miller's Theorem.

c) Design a self bias circuit using JFET for $I_D = 3mA$, $V_{DD} = 20V$ and $V_{DS} = 0.6 V_{DD}$.
($I_{DSS} = 8mA$, $V_P = -4V$)

d) Explain various types of capacitors.

e) Determine the values of coupling capacitors C_{C1} and C_{C2} if $r_{\pi} = 1.5K\Omega$, $\beta = 120$ and $f_L = 20Hz$.



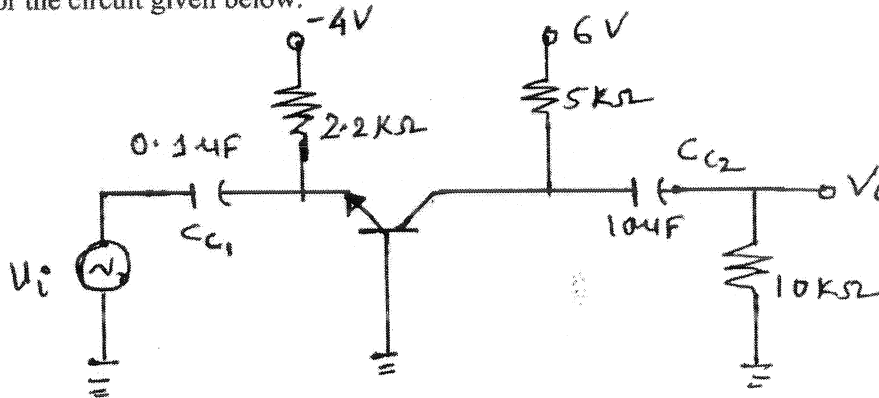
f) Explain concept of zero temperature drift in JFET.

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Q2. A) Calculate 1) I_{BQ} , I_{CQ} 2) g_m , r_{π} 3) Small signal voltage gain

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For the circuit given below.



Q2 B) Explain the concept of LC filter in power supply circuit and hence derive expression for ripple factor of LC filter.

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Q3 A) Explain concept of shunt Zener regulator. For a shunt Zener regulator giving

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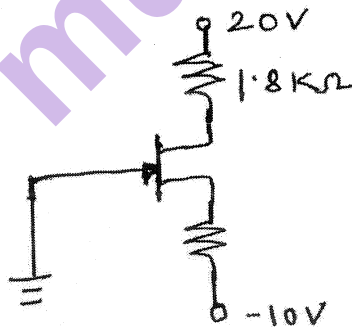
output voltage of 10 V and load resistance varying from 5 kOhm to 10 kOhm, V_{in} is varying between 18V to 22V.

Find R_s , P_{zmax} , S_v and R_o .

Assume $R_z = 4\Omega$ and $I_{zmin} = 50\mu A$.

B) Determine I_{DQ} , V_{GSQ} , V_{DSQ} if $I_{DSS} = 9mA$ and $V_p = -3V$ for the circuit given below.

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Q4 A) Design capacitive filter with FWR using two diodes with ripple factor less than 5%.

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Output voltage is 24V and load current 200mA. The input line voltage of 230V/ 50Hz is available.

B) Determine the values of biasing components for a CE configuration if $V_{CC} = 12V$, $V_{CE} = 6V$, $R_c = 1k\Omega$, $V_{BE} = 0.6V$, $\beta = 180$ for the following circuit.

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i) Fixed bias without R_E

ii) Voltage Divider bias with $V_{RE} = 10\%$ of V_{CC} and $S_1 = 8$

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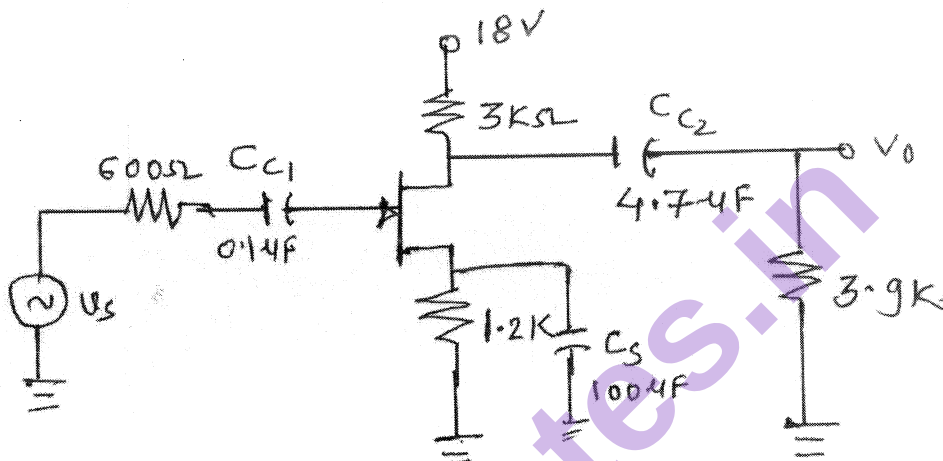
Q5 A) For JFET if $I_{DSS} = 6 \text{ mA}$, $V_P = -6 \text{ V}$, $r_d = \infty$, $C_{gd} = 4 \text{ pF}$, $C_{gs} = 6 \text{ pF}$, $C_{ds} = 1 \text{ pF}$ 15

Determine i) V_{GSQ} ii) I_{DQ}

iii) g_{mo} iv) g_m

v) Midband voltage gain A_v

vi) Higher cut off frequency



B) Explain high frequency π equivalent model of common emitter BJT.

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Q6. Design single stage CS amplifier using mid-point biasing method for voltage gain of 12, 20

$F_L = 20 \text{ Hz}$, $R_L = 10 \text{ K}\Omega$, $V_O = 3.5 \text{ V}$

(Use JFET parameters $I_{DSS} = 7 \text{ mA}$, $V_P = -2.5 \text{ V}$, $g_{mo} = 5600 \mu\text{S}$, $r_d = 50 \text{ K}\Omega$)