University of Mumbai
Examination May-June 2022

Program: **Electronics Engineering**

Curriculum Scheme: Rev2016

Examination: BE Semester VIII

Course Code: ELX802 and Course Name: AnalogandMixedVLSIDesign

Time: 2 hours 30Minutes Max. Marks: 80

==========

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks 20 Marks**
1.	In current mirror circuit, the first MOSFET (which copy current from reference) is operating in which region?
Option A:	Linear
Option B:	Saturation
Option C:	Cut-off
Option D:	deep triode region
2.	Which of the following statement is true in case of Base to Emitter voltage (V_{BE}) of BJT?
Option A:	It has negative temperature coefficient
Option B:	It has positive temperature coefficient
Option C:	It has both temperature coefficient
Option D:	It is equal to $(I_B)^2$
3.	The condition for MOSFET to be in deep triode region is----------.
Option A:	$V_{DS} << 2(V_{GS}-V_{TH})$
Option B:	$V_{DS} >> 2(V_{GS}-V_{TH})$
Option C:	$V_{DS} << (V_{GS}-V_{TH})$
Option D:	$V_{DS} >> (V_{GS}-V_{TH})$
4.	Thermal noise is generated from MOSFET by ----------
Option A:	Conduction of charge carriers in the channel
Option B:	Electric field across the gate and channel
Option C:	Capacitance of the gate oxide
Option D:	Substrate bias effect
5.	CS amplifier with Source degeneration voltage gain
Option A:	increases
Option B:	decreases
Option C:	moderate
Option D:	zero

6.	ro is the internal resistance of a MOSFET is equal to
Option A:	$1/\lambda I_D$
Option B:	λ/I_D
Option C:	I_D/λ
Option D:	λI_D
7.	In Switched Capacitor circuits, to achieve a higher sampling speed, _____& _____must be used.
Option A:	A small aspect ratio, a small capacitor
Option B:	A Large aspect ratio, a large capacitor
Option C:	A small aspect ratio, a large capacitor
Option D:	A Large aspect ratio, a small capacitor
8.	Which of the following is the main advantage of semicustom design approach over full custom design?
Option A:	Use of standard cells to reduce design time and complexity
Option B:	High performance
Option C:	More complexity
Option D:	High Speed
9.	What is the function of low pass filter in phase-locked loop (PLL) circuit?
Option A:	Improves low frequency noise
Option B:	Removes high frequency noise
Option C:	Tracks the voltage changes
Option D:	Changes the input frequency
10.	The resolution of 8-bit DAC/ADC is_____
Option A:	562
Option B:	256
Option C:	625
Option D:	128

Q2	**Solve any Four out of Six 5 marks each**
A	Explain trade-offs in analog design with the help of analog design octagon.
B	What are the disadvantages of basic current mirror circuit and how it is overcome in cascode current mirror?
C	Explain the concept of switched capacitor circuit.
D	Which errors are contributed by charge injection mechanism in MOS sampling circuits?
E	Compare performance parameters of various op-amp topologies.
F	Explain behaviour of g_m as function of below parameters 1. Overdrive voltage with W/L constant. 2. Overdrive voltage with I_D constant

Q3	Solve any two out of three 10 marks each
A	Derive the expression of voltage gain and output resistance of the source follower circuit.
B	What is a bandgap reference? Describe methods of implementation of band gap references.
C	Explain AMS design flow in VLSI circuit. Compare full custom and semi-custom design.

Q4	Solve any two out of three 10 marks each
A	Draw and explain charge pump PLL circuit
B	What are the various types of ADC architectures? Explain any two architectures in detail.
C	Derive the equation of Differential gain and Common mode gain of differential amplifier.