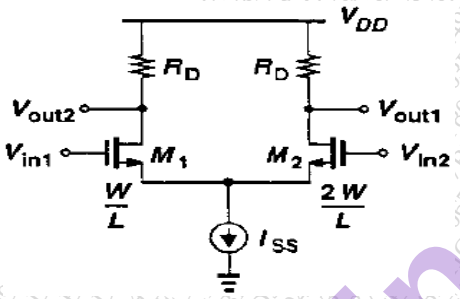
Time: 3 Hours Max Marks: 80

N.B. 1) Question No.1 is compulsory
2) Solve any three questions from the remaining questions.
3) Assume suitable data if necessary.

1 Solve the following.

(a) Analyze following circuit to get voltage gain equation if M2 is twice wide as that of M1 and Vin1=Vin2 5



(b) Explain the concept of switched capacitor circuit 5

(c) Compare performance of various op-amp topologies 5

(d) Explain System on Chip and System in Package. 5

2 (a) Design two stage operational amplifiers that meet the following specifications with a phase margin of 60. Assume the channel length is to be 1µm, KN'=100µA/V2, KP'= 20µA/V2, VTN = |VTP| = 0.5V, λ_N = 0.06V-1, and λ_P = 0.08V-1 Av>5000v/v, Vdd=2.5V, Vss= -2.5v ,GBW=5MHz , C_L=10pf , SR>10v/µsec, Vout range=+/- 2V, ICMR= -1 to 2V, $P_{diss} \leq$ 2mw.. 20

3 (a) Derive expression for voltage gain AV and output resistance Ro of source follower stage. 10

(b) Compare full custom and semi-custom design in terms of its trade-off and applications. 5

(c) Explain Non-ideal effects in PLL. 5

4 (a) Derive equation of differential gain, common mode gain and CMRR of differential amplifier. 10

(b) Explain White & Flicker noise in MOSFET. Derive equation for output and input referred noise voltage of CS stage 10

5 (a) Draw and explain AMS design flow. 10

(b) Draw and explain discrete time integrator along with the output waveform. 10

6 Write short note on **any four**

(a) Band Gap references 5

(b) Cascode current mirror circuit. 5

(c) Advantage and disadvantages of DLL 5

(d) Stability and frequency compensation of two stage Opamp 5

(e) Performance parameters of VCO 5

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