

(3 Hours)

Total Marks: 80

- N.B. 1) Question No.1 is compulsory
 2) Solve any three questions from the remaining questions.
 3) Assume suitable data if necessary.

1. Answer any four:
 - (a) Describe bonded SOI and smart cut SOI method 5
 - (b) Enlist the steps for obtaining Si from sand. 5
 - (c) What is short channel effect? How to avoid it? 5
 - (d) Explain any one application of nanowire 5
 - (e) Explain difference between positive and negative photo resist 5
2. (a) Explain Liquid phase epitaxy method. What are its advantage and disadvantage? 10
 - (b) Explain RCA cleaning method. 5
 - (c) State comparison of APCVD, LPCVD and PECVD. 5
3. (a) Enlist step for fabrication of CMOS inverter using N well process. Draw vertical cross sectional view starting from substrate till the gate, source and drain formation in fabrication of CMOS inverter. 10
 - (b) Draw layout of 2 input CMOS NAND gate using lambda based design rule 10
4. (a) Describe with help of neat diagram of Hynes schokley experiment for measurement of drift mobility of n type semiconductor 10
 - (b) Explain Deal and Groove model for oxidation 5
 - (c) Explain BiCMOS 5
5. (a) What is LOCOS? Why it is required in CMOS process. Explain technology solution for avoiding problem in LOCOS. 10
 - (b) Explain Difference between schottky contact and ohmic contact 5
 - (c) Explain Difference between Dry etching and Wet etching 5
6. Write short notes 20
 - (a) MODFET devices
 - (b) Multigate device structure
 - (c) High k and low k dielectric
 - (d) Need of lambda based design rule
 - (e) X ray lithography