

(Time:3 Hours)

Total Marks: 80

Note: 1) Question No.1 is compulsory.**2) Attempt any three questions from remaining five questions.****3) Assume suitable data if necessary.****4) Figures to the right indicate full marks.**

- Q.1) Explain in brief
- a) EDLC 5M
 - b) SPI 5M
 - c) Semaphores 5M
 - d) Task states 5M
- Q.2) a) What is the necessity of task scheduling? Explain Task Switching. 10M
Three periodic processes scheduled using EDF, will processes meet the deadlines?
- | Process | Execution Time = e_i | Period = p_i |
|---------|------------------------|----------------|
| P1 | 1 | 8 |
| P2 | 2 | 5 |
| P3 | 4 | 10 |
- b) Suggest the various strategies to help faster programming. 10M
- Q.3) a) What is priority inheritance problem? Explain it with neat sketch. Suggest solutions. 10M
- b) What need is of debug and trace facility? How cortex M3 supports it? 10M
- Q.4) a) Design G+ n an elevator system. Give the proper details for this, 10M
- i. FSM which describes the functioning of the system
 - ii. Hardware block diagram and list of components with justification
 - iii. Design challenges and suggest solutions for ethical practice in development
- b) Explain various design metrics. Explain the various optimization challenges for embedded system. 10M
- Q.5) a) What are different communications means available for industrial field devices? 10M
- b) Explain briefly register structure of Cortex M3 architecture along with the function of various special registers. 10M
- Q.6) a) Give the comparison details between black box and white box testing. 10M
- b) Write short note on: i) Various data types ii) FPGA 10M