University of Mumbai

Examinations Summer 2022

Time: 2 hour 30 minutes Max. Marks: 80

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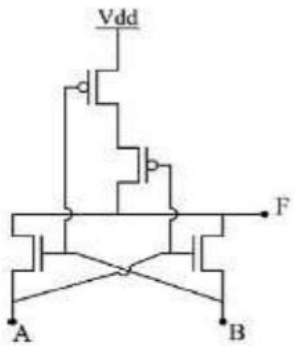
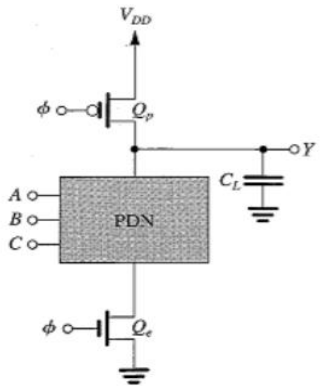
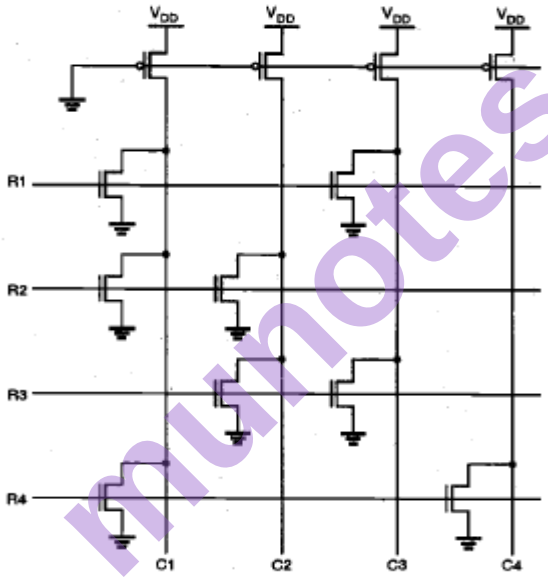
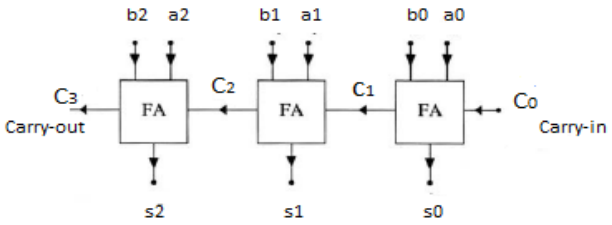
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1	Which condition is true for scaling factor S:
Option A:	S<1
Option B:	S=1
Option C:	S=0
Option D:	S>1
2	If the Noise Margin of the circuit increases then Noise Immunity
Option A:	Increases
Option B:	Decreases
Option C:	No change
Option D:	All of the above
3	How many MOS require for designing 2-i/p NAND Gate using static CMOS Design Style.
Option A:	NMOS-1, PMOS-2
Option B:	NMOS-2, PMOS-2
Option C:	NMOS-1, PMOS-1
Option D:	NMOS-2, PMOS-1
4	For a symmetric CMOS inverter, which condition is true?
Option A:	$(W/L)_P = 1.5\ (W/L)_N$
Option B:	$(W/L)_N = 1.5\ (W/L)_P$
Option C:	$(W/L)_P = 2.5\ (W/L)_N$
Option D:	$(W/L)_N = 2.5\ (W/L)_P$
5.	CMOS domino logic is the same as _____ with an inverter at the output line.
Option A:	clocked CMOS logic
Option B:	dynamic CMOS logic
Option C:	gate logic
Option D:	switch logic
6	In the circuit shown, A and B are the inputs and F is the output. What is the functionality of the circuit? 
Option A:	XOR
Option B:	SRAM Cell
Option C:	Latch

Option D:	NOR
7	Following diagram represents which design style : 
Option A:	CMOS Domino Logic
Option B:	CMOS static logic
Option C:	Pass transistor logic
Option D:	CMOS Dynamic Logic
8	In the following circuit if R1, R2, R3, R4 logic level is 0001 then C1,C2,C3,C4 logic level will be 
Option A:	0101
Option B:	0011
Option C:	0110
Option D:	1001
9	All DRAM requires periodic refreshing of data because
Option A:	Stored data can be modified
Option B:	Data stored as charge in a capacitor can't be retain indefinitely
Option C:	Stored data can be erased
Option D:	Data can be written in memory

10.	 Adder circuit shown in the above fig. is..... where a_n and b_n are input bits and C_n & S_n arecarry and sum respectively.
Option A:	3bit Carry look ahead adder
Option B:	4 bit Carry look ahead adder
Option C:	3 bit Ripple Carry Adder
Option D:	4 bit Ripple Carry Adder

Q2	**Solve any Four out of Six** **5 marks each**
A	Compare Bipolar, NMOS and CMOS technologies.
B	Compare SRAM and DRAM.
C	Design a 4:1 MUX using nMOS pass transistor logic.
D	Draw VTC of CMOS inverter. Show all critical voltages in it.
E	Compare Static CMOS, Dynamic CMOS and Pseudo nMOS logic.
F	Explain basic Manchester Carry Circuit with suitable diagram.

Q3	**Solve any Two Questions out of Three** **10 marks each**
A	Calculate noise margin of a CMOS inverter with the given parameters: NMOS $V_{To,n}$=0.6V , k_n=200uA/V^2, PMOS $V_{To,p}$=-0.7V , k_p=80uA/V^2, V_{DD}= 3.3V.
B	Implement the following function $Y=\overline{(A+B)(C+D)E}$ using: I) Static CMOS Logic II) Dynamic CMOS Logic III) Pseudo nMOS Logic
C	Draw 6T SRAM cell structure using MOS. Explain read, write and hold operations in detail.

Q4	
A	**Solve any Two** **5 marks each**
i.	Design a 4*4 NAND based ROM, which stores the following words: Row(0) 1000 Row(1) 1111 Row(2) 0111 Row(3) 1110
ii.	Design a half adder using Transmission Gate logic.
iii.	Compare Constant Voltage scaling and Full scaling with respect to following MOS parameters: Oxide Capacitance, Packing Density, Power Dissipation, Drain current and Saturation Current.
B	**Solve any One** **10 marks each**
i.	Explain 4 bit CLA adder with its carry equation. Draw the logical network using dynamic CMOS logic.
ii.	Design Master slave JK Flip Flop using any MOS Design Style.