Time: 3 Hours **Max Marks: 80**

N.B: 1) Question no. 1 is compulsory.
2) Attempt any three out of the remaining five questions
3) Use suitable data, wherever necessary.

Q 1: Attempt any four questions from the following: **(20)**

a. Explain the function of given CPU registers used in Von Neumann model:
MAR, MDR, IR, PC, SP

b. Differentiate between DRAM and SRAM

c. Why does a superscalar processor use dynamic branch prediction? Justify.

d. Define Micro-operation, Microinstruction, Micro-program, Micro-code.

e. In a multiprocessor system, suppose an application runs on a 4-processor machine and 80% of the application is parallelizable, compute the achievable speedup by applying Amdahl's law.

Q 2 (a) Show the multiplication process using Booth's algorithm and multiply the following:
Multiplicand = +23
Multiplier = - 6 **(10)**

Q2 (b) Explain cache memory mapping techniques with an example **(10)**

Q3(a) Demonstrate the advantages of pipelining and explain various types of pipeline hazards and their solutions. Give examples **(10)**

Q3(b) Explain in detail hardwired control. Discuss any one method to implement it. **(10)**

Q 4(a) Explain page replacement algorithm also find out page faults, page hit, hit ratio for the following string using FIFO and LRU method. Consider page frame size = 3.
2 3 8 9 5 3 8 5 3 3 1 2 4 8 5 4 **(10)**

Q 4(b) Explain in detail, different types of buses and methods of arbitration. **(10)**

Q 5(a) Explain in detail, characteristics of RISC and CISC **(10)**

Q 5(b)Explain Flynn's classification for parallel processing systems. **(10)**

Q 6. Write short notes on (any four) **(20)**

a. IEEE 754 format
b. PCI bus Architecture
c. NUMA
d. Cluster computing
e. Control sequence for the execution of SUB R1, (R2) instruction.
