(3 Hours) **(Total Marks : 80)**

N.B.: 1) **Question No.1** is **compulsory**.
2) Attempt **any three** questions from remaining questions.
3) **Figures** to the **right** indicate **full marks**.

Q1.	(a)	Explain IEEE 754 format for 32 bit numbers	**5**
	(b)	How does cache memory improve system performance?	**5**
	(c)	Write short notes on nano programming	**5**
	(d)	Write short notes on memory hierarchy	**5**
Q2.	(a)	Explain Booth's algorithm. Solve 6*5 using Booth's algorithm. 5 is multiplier	**10**
	(b)	Draw the flowchart for restoring division algorithm. Solve 9 ÷ 4 using restoring division algorithm	**10**
Q3.	(a)	What is microprogramming? Draw and explain microprogrammed control unit	**10**
	(b)	Explain hardwired control unit with a neat diagram. Describe clearly the generation of control signals with examples	**10**
Q4.	(a)	Explain the paging mechanism. State advantages of paging and the importance of the translation lookaside buffer (TLB) in paging.	**10**
	(b)	Consider a 2-way set associative mapping with block size =16 bytes, cache size=16k main memory size =256k. Design a cache structure and show how the processor address is interpreted..	**10**
Q5.	(a)	State the advantages of pipelining. Explain any two types of pipeline hazards and their solutions.	**10**
	(b)	What is the necessity of a replacement algorithm? Explain how pages are replaced using LRU and LFU algorithms	**10**
Q6.	(a)	Briefly explain programmed I/O, interrupt driven I/O and DMA	**10**
	(b)	Explain with examples any five addressing modes of IA32 processors	**10**

2337C0CD50FE594F32A7EB635D0C98C5