Time: 3 Hours   **Total Marks: 80**

N. B. : (1)   Question No. 1 is compulsory.
    (2)   Attempt any three out of remaining.
    (3)   Assume suitable data wherever required.

Q.1   Solve the following (Any four)   **20 Marks**
    A. Explain the necessity of randomization in system Verilog.
    B. Explain the conditional coverage and branch coverage with suitable example.
    C. Short note on semaphores and describe their use in System Verilog with suitable
        example.
    D. List the advantages of assertions in system Verilog.
    E. Differentiate between FPGA and CPLD.

Q.2   A. Discuss Silicon technology challenges.   **10 Marks**
    B. Explain various types of arrays used in System Verilog.   **10 Marks**

Q.3   A. Explain the necessity and advantages of using interface.   **10 Marks**
        Elaborate with example.

    B. Explain various data types in Verilog? Write Verilog code to swap **10 Marks**
    contents of two registers with and without a temporary register?

Q.4   A. Draw and explain each block of Layered testbench used in verification.   **10 Marks**
    B. What are different types of coverage? Explain line and toggle coverage   **10 Marks**
        with suitable example.

Q.5   A. List the methods of interprocess communication. Explain ant two in detail. **10 Marks**
    B. What is the significance of program block?   **10 Marks**
        For the interface, write the code for:
        1. A clocking block that is sensitive to the negative edge of the clock and all I/O that are
            synchronous to the clock.
        2. A modport for the testbench called master and a modport for the DUT called slave.
        3. Use the clocking block in the I/O list for the master modport

Q.6   A. Explain various Fork Join statements supported in System Verilog.   **10 Marks**
    B. Describe immediate and concurrent assertions in detail.   **10 Marks**

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