(3 Hours) **[Total Marks: 80]**

N. B. : (1) Question No. 1 is compulsory.
(2) Attempt any three out of remaining.
(3) Assume suitable data wherever required.

Q.1 Solve the following **(Any four)** **20**

A. Explain the usage of Modport in System Verilog Interface.
B. Differentiate between Blocking and Non blocking assignments in Verilog with proper example.
C. What is verification or test plan. Write the test plan for ALU design.
D. Differentiate directed testing and random testing concepts.
E. What are the advantages of OOP in System Verilog?

Q.2 A. Highlight the 4 modelling styles used in Verilog. Write Verilog code for full adder using two half adders. **10**

B. **10**

i. Declare Dynamic array. Allocate 5 elements. Print out its size.
ii. Declare a Queue and initialize it with 5 string element. Insert new element @position 2.
iii. Is Logic datatype in SV 2-state or 4- state? How it is different than wire.
iv. Create Enumerated data type for all rainbow colours.
v. Declare 2D array. Display each & every element of it using **foreach.**

Q.3 A. Draw the layered test bench diagram and explain each of blocks stating its functionality. **10**

B. Create a class called TE_semV that contains the following members: **10**

3-bit roll_no of logic type
student_name of string type
4-bit address of logic type
A void function that prints out the value of roll_no, name and address

i. Initialize address to 4'hF in the 1st object, passing arguments by name
ii. Initialize roll_no to 3 and name to Sumanto in the 2nd object, passing arguments by name.
iii. Use the print function to print out the values of roll_no and name for the 2 objects.

Q.4 A. Explain the concept of randomization and why it is required in design verification. **10**

B. What is coverage and cross coverage? List and explain all types of Code coverage? **10**

Q.5 A. Explain immediate and concurrent assertions in detail. **10**

B. Write the System Verilog code for the following items: **10**

1) Create a class Exercise1 containing two variables, 8-bit data and 4-bit address. Create a constraint block that keeps address to 3 or 4.

2) Modify the above code for so that:

data is always equal to 5
Probability of address = 4'd0 is 10%
Probability of address being between [1:14] is 80%
Probability of address = 4'd15 is 10%

Demonstrate its usage by generating 20 new data and address values and check for error.

Q.6 A. Explain various Fork Join statements supported in System Verilog with proper examples. **10**

B. Write all the methods associated with Events, Semaphores and mailbox. Mention the function of each of the methods and give example? **10**
