[Time: 3Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. **Question no. 1 is compulsory.**
2. **Attempt any three out of the remaining five questions.**
3. **Use suitable data, wherever necessary**

Q1 Attempt (**any 4**)

A. Implement EX-OR gate using only NAND gates. **05**

B. Explain FAN in, FAN out, power dissipation and noise immunity with reference to Digital lC's. **05**

C. Explain glitch problem of ripple counter. **05**

D. Write a note on VHDL Framework. **05**

E. Draw the truth table and logic diagram of Full Subtractor.

Q2 A Draw a circuit diagram of two input TIL NAND gate and explain its operation. **10**

B Design 4 bit Johnson counter using J-K Flip Flop. Explain it operation using waveform. **10**

Q3 A Design a circuit with optimum utilization of PLA to implement the following functions. **10**

$F1 = \sum m(0,2,5,8,9,11)$

$F2 = \sum m(1,3,8,10,13,15)$

$F3 = \sum m(0,1,5,7,9,12,14)$

B Eliminate redundant states and draw reduced state diagram. **10**

PS	NS		O/P
	X=0	X=1	Y
A	B	C	1
B	D	F	1
C	F	E	0
D	B	G	1
E	F	C	0
F	E	D	0
G	F	G	0

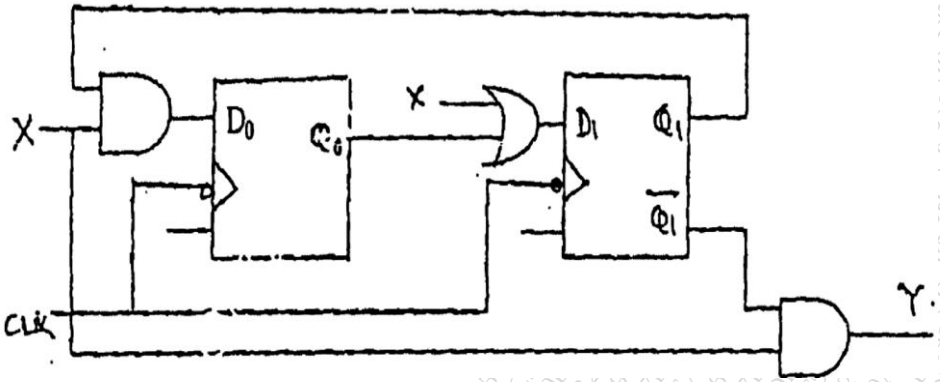
Q4 A Implement the function using single IC 74151 and some gates. **10**

$F = \sum m(1,2,4,7,10,13,14)$

10

B Design asynchronous Mod-8 counter using T-Flip flop.

Q5 A Analyze the sequential state machine shown in figure. Obtain state diagram for the same. **10**



B) Design a mod-16 up counter using IC 74163, draw the circuit diagram and explain its working. **10**

Q6 Write notes on. **20**

1. Stuck at '0' and Stuck at '1' faults.
2. XC 4000 FPGA Architecture
3. Master Slave JK Flip Flop
4. Mealy and Moore Sequential Machine
