

Time: 3 Hours**Max Marks:80**

- N.B: 1) Question no. 1 is compulsory.
 2) Attempt any three out of the remaining five questions
 3) Use suitable data, wherever necessary.

Que 1 : Attempt any four questions from the following. (20 M)

- I. Compare TTL and CMOS Logic families with respect to
 - i) Power dissipation ii) Propagation delay iii) Figure of merit iv) Fan-out
- II. Convert $(73.301)_{10}$ into binary, octal, Hexadecimal and BCD equivalent.
- III. Simplify following three- variable expression using Boolean algebra
 $\prod M(0, 1, 3, 4, 7)$
- IV. Design Half adder circuit using basic gate.
- V. Explain different types of triggering methods used for flipflop

Que 2 A) Perform following operation: (10 M)

- i) Addition $24_{BCD} + 18_{BCD}$ ii) Subtraction $46_{10} - 22_{10}$ using 2's complement method

Que 2 B) Reduce the given expression and Realize using NAND gate only. (10 M)

$$Y = AB' + AC' + C + AD + AB'C + ABC$$

Que 3 A) Simplify the following function using Quine-Mccluskey method.

$$\sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11)$$

Que 3 B) Design 2 Bit Magnitude comparator using gates (10 M)

Que 4(A) Implement the following Boolean function with 8:1 Multiplexer (10 M)

$$F(A, B, C, D) = \sum m(0, 2, 6, 10, 11, 12, 13) + \sum d(3, 8, 14)$$

Que 4(B) Draw and explain working of Bidirectional shift register. (10 M)

Que 5(A) Design MOD 13 Asynchronous up counter using JK Flip flop (10 M)

Que 5(B) Convert JK Flip flop into D and SR flipflop (10 M)

Que 6 (A) Design 3 bit Synchronous counter using T flip flop (10 M)

Que 6(B) Explain Race around condition in JK flipflop and discussion solution to avoid Race around condition (10 M)