[Time: 3Hours] **[Marks:80]**

N.B:
1. **Question No. 1 is compulsory.**
2. **Out of remaining questions, attempt any THREE questions.**
3. **Assume suitable data, wherever necessary.**

Q1 Attempt **any Four:** **20**

a) Construct 2-input EX-OR and EX-NOR Gates using only NAND gates.
b) Differentiate between Combinational and Sequential Circuits.
c) Write truth table and draw logic diagram of Half Adder.
d) Explain any five features of VHDL.
e) Design MOD-6 counter using IC 7490.

Q2 a Simplify F = II M (0,2,5,8,10, 12, 15) + d (1,6) using K-map. **10**
Implement the function using only NOR gates.

b Design 8-bit comparator using four bit magnitude comparator IC 7485. **10**

Q3 a Design Mod-8 synchronous counter using JK flip-flop. Draw output Waveform. **10**

b Eliminate the redundant states and draw the reduced state diagram. **10**

PS	**NS**		**O/P**
	X=0	X=1	Y
A	B	C	1
B	D	C	0
C	F	E	0
D	E	B	1
E	B	C	1
F	C	E	0
G	F	G	0

Q4 A Implement F_1 (A, B, C) = $\sum$ m (0,2,4,7) **10**
F_2 (A, B, C) =$\sum$ m (1,2,5,7)
Using IC 74151, 8:1 Multiplexer.

b Design a mealy sequence detector to detect ----10l l -----using D flip-flops, Wherein overlapping is allowed. **10**

Q5 a List out different types of PLD's. Implement the given functions using PLA. **10**
F1 (A,B,C) = $\sum$ m (3,6, 7) F2(A,B,C) = $\sum$ m (1,2,4, 7)

b Draw neat diagrams of 2-input TTL NAND gate and explain in brief. **10**

Q6 Write short notes on (**any Four**) **20**

a) CPLD Architecture
b) Stuck at 0 &1 Faults
c) Johnson Counter & its applications
d) State Assignment Techniques
e) JK-Flip flop