Time: 3 Hrs **Marks: 80**

NB: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of **remaining five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

Q.1 Answer Any Four.

a) Convert the decimal number $(175.23)_{10}$ to their octal, hexadecimal, BCD and gray code equivalent. **5m**

b) Prove the following Boolean theorem. **5m**
$(A+\bar{A}B) = (A+B)$

c) Implement CMOS inverter and NOR gate. **5m**

d) Design and implement half subtractor circuit. **5m**

e) Explain various triggering methods and symbols of flip flops. **5m**

Q.2 a) Simplify the logic function using Quine-McClusky method. **10m**
$Y (A, B, C, D) = \Sigma m (0 ,1,2,3,5,7,8,9,11,14)$
b) Design and implement D flip flop using T flip flop and JK flip flop using D flip flop. **10m**

.Q.3 a) Design and implement asynchronous MOD-9 counter using T flip flop. **10m**
b) Draw and explain 5bit comparator using IC 7485. **10m**

Q.4 a) Implement and explain 4-bit BCD adder using IC 7483. **10m**
b) Design and implement the following expression using a single 8:1multiplexer . **10m**
$Y (A, B, C, D) = \Sigma m (0 ,2,3,6,8,9,12,14)$

Q.5 a) Draw and explain master slave JK flip flop with its advantage. Derive characteristics equation and excitation table of JK flip-flop. **10m**
b) Implement and explain 4-bit twisted ring counter. **10m**

Q.6 Write a short note on **any three.** **20m**
a) Hamming code
b) Characteristics of logic families
c) Static and dynamic Hazards
d) Application of flip flop in switch debouncing

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