( 3 Hours ) Marks : 80

NB : (1) Question **No.1** is **compulsory.**
(2) Out of remaining questions, attempt **any three** questions.
(3) Assume suitable data, wherever necessary.

1. (a) Explain the term noise margin and its value for TTL and CMOS family. **5**
(b) Differentiate between synchronous and asynchronous counter. **5**
(c) Draw truth table and logic diagram of Full Adder. **5**
(d) Explain shift registers and its applications. **5**

2. (a) Use k- map to reduce the following function and then implement it using NOR gates only. **10**
$F(ABCD) = \sum m(4,6,12,14) + \sum d(1,3,9,11)$
(b) Implement the following function using 8:1 MUX and logic gates. **10**
$P(A,B,C,D) = \sum m(1,2,5,8,10,12,15) + \sum d(0,6)$

3. (a) Design a mealy sequence detector to detect 1010 using D flip-flops and logic gates. **10**
(b) Design a MOD 5 asynchronous counter and explain the glitch problem. **10**

4. (a) Design a circuit with optimum utilization of PLA to implement the following functions. **10**
$F1 = \sum m(2,12,13)$
$F2 = \sum m(7,8,9,10,11,12,13,14,15)$
$F3 = \sum m(1,2,8,12,13)$

(b) Design 4 bit Johnson counter using J-K flip-flop. Explain its working using waveform. **10**

5. (a) Eliminate redundant states and draw reduced state diagram. **10**

| Present State | Next State | | Output | |
|---|---|---|---|---|
| | X = 0 | X = 1 | X = 0 | X = 1 |
| 1 | 2 | 3 | 0 | 0 |
| 2 | 2 | 4 | 0 | 0 |
| 3 | 2 | 3 | 0 | 0 |
| 4 | 5 | 3 | 0 | 0 |
| 5 | 2 | 6 | 0 | 1 |
| 6 | 5 | 3 | 0 | 0 |

(b) Discuss XC 4000 FPGA architecture with neat block diagram. **10**

**[TURN OVER**

6. Write notes on : **20**
   (a) VHDL
   (b) Stuck at '0' stuck at '1' fault.
   (c) Master slave JK flip-flop.
   (d) BCD Adder.

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