University of Mumbai

Examinations First Half 2022

Program: **Electrical Engineering**
Curriculum Scheme: Rev2019
Examination: SE Semester IV
Course Code: EEC403 and Course Name: Digital Electronics

Note: 1. Make any suitable assumption

2. Figure to the right indicates full marks **Max. Marks 80**

Solve all.

Q1. **Choose the correct option for following questions. All the Questions are compulsory and carry equal marks** **(20)**

1 The MSB of signed binary number indicates its

Option A: parity

Option B: Sign

Option C: maximum number

Option D: its always zero and does not indicate any thing

2 The number of similar gates which a gate can drive is known as

Option A: output

Option B: fan out

Option C: drive capacity

Option D: A gate does not drive another gate

3 What is the BCD code for $(13)_{10}$?

Option A: 00001101
Option B: 00000111
Option C: 00010011
Option D: 00001011

4 Minimum number of selection inputs required for selecting one out of 32 inputs is --------

Option A: 4
Option B: 3
Option C: 5
Option D: 8

5. A three variable expression with variables A, B, C is given as Y=AB+AC+ABC.

This expression is in which form?

Option A: Canonical POS Form
Option B: POS Form
Option C: SOP Form
Option D: Canonical SOP form

6. How many cells will be present in the K-map of f(A,B,C,D)=πM(2,4,6,7)

Option A: 4
Option B: 8
Option C: 12
Option D: 16

7 The complex programmable logic device contains several PLD blocks and _____

Option A: Field-programmable switches
Option B: AND/OR arrays
Option C: A global interconnection matrix
Option D: A language compiler

8. Which Flip Flop is used to overcome the Race-Around condition?

Option A: D Flip Flop
Option B: Master Slave J K Flip Flop
Option C: S R Flip Flop
Option D: T Flip Flop

9 Derive the Boolean expression for the logic circuit shown below

Option A: $ABCDE$
Option B: $[C(A+B)D+\bar{E}]$
Option C: $[[C(A+B)D]\bar{E}]$
Option D: $C(A+B)DE$

10. Which of the following is a combinational circuit?

Option A: Multiplexer
Option B: Registers
Option C: Counters
Option D: Latches

Q.No. 2 . Solve any Two

a. Convert the hex number A72E to equivalent binary, decimal, octal , BCD and Grey code

(10)

b. Design BCD to Excess 3 code converter using basic gates.

(10)

c. Simplify the following using K-map implement using NAND gates
y = ∑ m (0,1,2,5,9,13,14,15) +d(4,6,10)

(10)

Q.No. 3. Solve any Two

a. Design MOD 12 synchronous counter using T flip flop. (10)

b. Explain the design of a 4 bits D to A converter using weighted register D/A technique. Use suitable diagrams for the explanation. (10)

c. Write a note on Programmable Arrey Logic. Implement the following using PAL $F(A,B,C,D) = \sum m(0,1,3,15)$ (10)

Q.No. 4. Solve any Two

a. i. Write a short note on memory mapping and address decoding.
ii. Write short notes on different logic families (TTL; CMOS). (10)

b. What is quantization? Explain three bits A to D converter using successive approximation technique. Explain with the help of suitable diagrams (10)

c. write short note on the characteristics of digital IC (10)