[Time: 3 Hours] [Marks:80]

Instructions:

1. Question no. 1 is **compulsory**.
2. Answer any **three** from remaining.
3. Figures to the **right** indicate **full marks.**

1. Answer any FOUR of the following **20**

i) Compare sequential and combinational logic circuits

ii) Draw circuit and derive expression for op-amp as as an adder and subtractor.

iii) Define the terms w.r.t op-amp i) Slew rate ii) input offset voltage

iv) Convert the following :
i) $(58)_{10}$ to Octal ii) $(275B)_{16}$ to binary

v) Explain interfacing between TTL and CMOS logic families.

2. a)Explain briefly the operation of TTL NAND gate in tristate output configuration **10**

b) Draw and explain operation of R-2R ladder DAC. Derive the expressions for its output voltage. State its advantages and disadvantages. **10**

3. a) Illustrate with neat circuit diagram, operation of Op-amp as an instrumentation amplifier. Derive the expression for output voltage **10**

b) Illustrate operation of Op-amp as basic integrator with circuit diagram. Draw input and output waveforms for input i) Triangular wave ii) square wave **10**

4. a) Implement the following SOP expression using i)Two 8:1 multiplexer ii) One 8:1 multiplexer **10**

$$f(A,B,C,D) = \Sigma m(0,2,3,4,6,9,10,12)$$ **10**

b) Design 3-bit synchronous counter using JK flip flops.

5. a) Minimize the expression using K-map and realize using gates. **10**

$$f(A,B,C,D) = \Sigma m(0,5,9,12,13,14,15) + d(1,2,3,4)$$

b) Design a 3-bit binary to gray code converter and implement using EX-OR gates. **10**

6. a) Design an astable multivibrator using IC 555 timer for 1 kHz frequency with 40% duty cycle. **10**

b) i) Simplify Y= $A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC + \bar{A}\bar{B}C$ and implement using basic gates.
ii) Implement EX-OR using NOR gates. **10**
