## **University of Mumbai**

## **Examination Summer 2022**

Time: 2 hour 30 minutes Max. Marks: 80

1. 8086 supports software Interrupts  Option A: 2  Option D: 64K  Option D: 8  2. In 8086 size of pre fetch queue is  Option A: 6 Byte  Option B: 4 Byte  Option C: 4 Bit  Option D: 2 Byte  3. The instruction that unconditionally transfers the control of execution to the specified address is  Option A: JMP  Option B: IRET  Option D: RET  Option D: CALL  4. In PUSH instruction, after each execution of the instruction, the stack pointer is incremented by 1  Option A: Incremented by 1  Option D: decremented by 2  5. stores the bits required to mask the IR lines of 8259  Option A: ISR  Option C: IRR  Option C: IRR  Option D: IRR  Option D: IRR  Option D: IRR  Option D: IRR  Option C: IRR  Option D: IRR  Option D: IRR  Option D: IRR  Option C: IRR  Option D: IRR  Option C: IRR  Option D: IRR  Option C: IRR  Option D: IRR  Option D: IRR  Option C: DACK  Option D: INTA   Which control registers of 80386 are associated with paging mechanism?  Option A: CRO, CR2, CR3	Choose the correct option for following questions. All the Questions are				
Option A: 2 Option B: 64K Option C: 256 Option D: 8  2. In 8086 size of pre fetch queue is Option A: 6 Byte Option C: 4 Bit Option D: 2 Byte  3. The instruction that unconditionally transfers the control of execution to the specified address is Option A: JMP Option B: IRET Option C: RET Option D: CALL  4. In PUSH instruction, after each execution of the instruction, the stack pointer is Option A: incremented by 1 Option B: decremented by 1 Option C: incremented by 2  Option D: decremented by 2  5. stores the bits required to mask the IR lines of 8259 Option A: ISR Option B: IMR Option C: IRR Option D: PR  6. The bus is available when the DMA controller receives the signal Option A: HRQ Option D: INTA  7. Which control registers of 80386 are associated with paging mechanism? Option A: CRO, CR2, CR3	Q1.	compulsory and carry equal marks			
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Option A: HRQ Option B: HLDA Option C: DACK Option D: INTA  7. Which control registers of 80386 are associated with paging mechanism? Option A: CR0, CR2, CR3	Option D:	PK			
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Option B: HLDA Option C: DACK Option D: INTA  7. Which control registers of 80386 are associated with paging mechanism? Option A: CR0, CR2, CR3					
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Option D: INTA  7. Which control registers of 80386 are associated with paging mechanism? Option A: CR0, CR2, CR3					
7. Which control registers of 80386 are associated with paging mechanism? Option A: CR0, CR2, CR3					
Option A: CR0, CR2, CR3	Option D.	INTA			
Option A: CR0, CR2, CR3	7.	Which control registers of 80386 are associated with paging mechanism?			
	Option A:				
νρων   O(\L) O(\L)	Option B:	CR1, CR2, CR3			
Option C: CR0, CR1 CR2					

Option D:	CRO, CR1 CR2,CR3
8.	How many flags are active in flag register of 80386?
Option A:	9
Option B:	12
Option C:	13
Option D:	10
9.	What lead to the development of MESI and MEI protocol?
Option A:	Cache size
Option B:	Cache Coherency
Option C:	Bus snooping
Option D:	Number of caches
10.	Hyperthreading uses the concept of
Option A:	Simultaneous multithreading
Option B:	Distributed decoding
Option C:	Multiple switching
Option D:	Pipelining

	Solve any Two Questions out of Three 10 marks each
Q2	
A	Explain and draw IVT? Differentiate between hardware and software interrupts?
В	Explain descriptors and paging mechanism in protected mode of 80386?
C	Explain the Initialization command words (ICWs) and Operational command words(OCWs) of the 8259 PIC.

Q3	Solve any Two Questions out of Three 10 marks each
A	Write an 8086 assembly language program to print the flag registers
В	Design 8086 microprocessor based system working in minimum mode with the following specifications.  I) 8086 microprocessor working at 8 MHz.  II) 16 KB EPROM using 8K devices.  Clearly show memory map with address range. Draw a neat schematic.
С	Explain protection mechanism of 80386 with diagram.

Q4	Solve any Two Questions out of Three 10 marks e	each
A	Draw and explain timing diagram of memory read and mer	mory
	write operation in minimum mode.	
В	Explain Pentium 4 Net burst micro architecture and write a note of	n
	hyperthreading	
С	Explain Integer and Floating-Point Pipeline of Pentium.	

