Time : 3 Hours **Max. Marks: 80**

N.B. (1) Question No. 1 is compulsory
(2)Assume suitable data if necessary
(3)Attempt any three questions from remaining questions

Q1 Attempt any four

a. Given the two binary numbers x=1010100 and y=1000011 perform the subtraction x-y, using 2's complement. (5)
b. Add $(57)_{10}$ and $(26)_{10}$ in BCD. (5)
c. Design Full Adder using logic gates. (5)
d. Compare TTL and CMOS logic families. (5)
e. Prove NAND as a universal gate. (5)

Q2 a. Explain the uses of grey code. (5)
b. Convert JK f/f into D f/f. (5)
c. Simplify using Quine Mc Clusky method F (ABCD)= $\sum$m (0,1,2,5,7,8,9,10,13,15). (10)

Q3 a. Design 3 bit synchronous down counter using suitable flip-flops. (10)
b. Design 4-bit BCD adder (10)

Q4 a. Solve using K map and implement using NAND gates only
F(ABCD) = $\sum$ m (1,2,3,8,9,10,11,14)+ d(7,15). (10)
b. Explain 4 bit bidirectional shift register. (10)

Q5 a. Write Short note on Priority Encoder. (5)
b. Sate and prove De Morgan's theorem. (5)
c. Design a 2-bit magnitude comparator. (10)

Q6 a. Compare synchronous and asynchronous counters. (5)
b. Implement full adder using 3 to 8 decoder and NAND gates. (5)
c. Explain Master Slave JK flip flop in detail. (10)

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