Paper / Subject Code: 50274 / Digital Logic & Computer Architecture

	(3 nours)			Total Marks: 8	
		N.B.	 Question No. 1 is compulsory Attempt any three questions from remaining five questions Assume suitable data if necessary and justify the assumptions Figures to the right indicate full marks 		
Q1	A	Diffe	rentiate between Computer organization and computer architecture	05	
	В	Draw	the flow chart for of Restoring division algorithm	05	
	C D		rentiate between Hardwired control unit and Micro programmed control unit IEEE 754 floating point representations.	nit 05 05	
Q2	A	Draw	the flow chart Booths algorithm for multiplication and Perform 6 X 2	5 10	
	В		ribe the detailed Von-Neumann Model with a neat block diagram	05	
	C	Expla	ain Cache coherence	05	
Q3	A	Expla	ain the different addressing modes.	10	
	B C		ne Instruction cycle and draw the state diagram of instruction cycle ain Bus arbitrations	05 05	
Q4	A	. V -	ain Micro instruction format and write a micro program for the instruction R_1 , R_2	10	
	В		ain Hardwired Control Unit and the various design methods associated with	th it. 10	
Q5	A	Expla	nin various Memory mapping techniques	10	
	В	Expla	nin the concept of Locality of reference	05	
	C	List &	Explain the Characteristics of Memory	05	
Q6	A	Expla	nin Flynn's classification.	10	
	В	Descr	ribe Instruction Pipelining and its hazards.	10	
