(3 hours) **Total Marks: 80**

N.B. 1. Question No. 1 is compulsory
2. Attempt any three questions from remaining five questions
3. Assume suitable data if necessary and justify the assumptions
4. Figures to the right indicate full marks.

Q1	A	Convert i) 147 in to binary ii) $(23A)_{16}$ in to Decimal iii) $(135)_8$ in to decimal iv) 234 in to BCD v) 23 in to gray code	05
	B	Write a short note on Encoder	05
	C	Differentiate between Hardwired control unit and Micro programmed control unit	05
	D	Differentiate between SRAM & DRAM	05
Q2	A	Draw the flow chart of Non Restoring division algorithm and Perform 4 ÷2	10
	B	Explain Flynn's classification	10
Q3	A	Explain the instruction cycle with the help of a neat state diagram	10
	B	Explain the various addressing modes	10
Q4	A	Using booths algorithm perform -5 x -3	10
	B	Represent -786.25 using IEEE 754 standards (both single and double precision format)	10
Q5	A	Explain different memory Mapping Techniques	10
	B	List & Explain the Characteristics of Memory	05
	C	What do you mean by cache coherence	05
Q6	A	Draw and explain 4 stage instruction pipelining and briefly describe the hazards associated with it	10
	B	Describe various Bus Arbitration methods	10

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