Subject:Computer Organization & Design

Class: FYCS **SEM-I**

Note: This is just a sample question bank for Theory examination

R. N	QUESTION	OPTION1	OPTION2	OPTION3	OPTION4	ANSWER
1	The _____ format is usually used to store data	BCD	Decimal	Hexadecimal	octal	BCD
2	A source program is usually in _____	Assembly language	Machine level language	High-level language	Natural language	High-level language
3	Primary memory also called _____	main memory	cache memory	secondary memory	random access memory	main memory
4	The _____ gate is an electronic circuit that gives a **high** output (1) only if all its inputs are high.	AND	OR	NOT	NAND	AND
5	A plus (+) is used to show the _____ operation.	AND	NAND	OR	NOR	OR
6	Total number of inputs in a half adder is _____	2	3	4	1	2
7	There are _____ cells in a 4-variable K-map	12	16	18	none of these	16
8	Don't care conditions can be used for simplifying Boolean expressions in___	example	terms	k-maps	latches	k-maps
9	_____ gate is design using AND and NOT gate.	NAND	NOR	EX-OR	EX-NOR	NAND
10	machine language is also called as _____	object code	offset code	compiler code	language code	object code
11	machine language are represented by ____	0's	1's	decimal	0's and 1's	0's and 1's
12	__converts the programs written in assembly language into machine instructions.	Machine compiler	Interpreter	Assembler	Converter	Assembler
13	The instructions like MOV or ADD are called as _____	OP-Code	Operators	Commands	None of the mentioned	OP-Code
14	which method adds data elements to a list	push	pop	queue	stack	push
15	FILO stands for____	final in last out	first in last out	first info last output	first info last output	first in last out
16	A register is a group of ____ that can store a one bit of information.	Register	flip flop	register file	d-flip flop	flip flop
17	IR stands for	index register	instruction register	information register	immediate register	instruction register
18	PC stands for	program counter	perform counter	programming counting	processor counter	program counter
19	DMA stands for	Direct memory Address	Direction Memory Address	Directed memory access	Direct Memory Access	Direct Memory Access
20	In ____, data is directly transferred from an input/output device to RAM or from RAM to an input/output device.	DMA	DAA	RAM	ROM	DMA
21	_____ section responsible for decoding and generating control signals which takes appropriate actions for execution section.	Fetch	execution	decode	register	Fetch
22	_____ controls all parts of computer system.	Fetch	execution	control unit	register	control unit
23	The Pentium Pro is optimized for running _____ code.	20 bit	16 bit	8 bit	32 bit	32 bit
24	The address bus of Petium Prois widened to _____ bits,	36 bits, 64 GB	36 bits, 36 GB	64 bits, 64 GB	64 bits, 36 GB	36 bits, 64 GB
25	giving its maximum addressibility of _____ of memory.					